



# EMULEX MICRO DEVICES

## FAST ARCHITECTURE SCSI CHIP

### FAS216/226/236 \*

#### FEATURES

- ❑ For Host Applications and 16-bit Peripheral Applications
- ❑ Supports ANSI X3T9.2 SCSI Standard, with SCSI-2 Fast Timing Requirements
- ❑ Asynchronous Data Transfer up to 7 MB/sec
- ❑ Synchronous Data Transfers up to 5 MB/sec and 10 MB/sec FAST
  - Programmable Synchronous Transfer Period
  - Programmable Synchronous Transfer Offsets up to 15 Bytes
- ❑ 24-Bit Transfer Counter
- ❑ Functions as Initiator or Target
- ❑ Up to 20 MB/sec DMA Burst Transfer Rate (10 Megatransfers Per Second)
- ❑ Pipelined Command Structure
- ❑ 16 Byte Data FIFO Between the DMA and SCSI Channels
- ❑ Implements SCSI Sequences without Microprocessor Intervention
- ❑ Parity Pass-Through on FIFO Data
- ❑ Part Unique ID Code
- ❑ On-Chip 48 mA Single-Ended SCSI Transceivers
- ❑ Interrupts Microprocessor Only When Service is Required
- ❑ Packaging
  - 216 - 84 PLCC
  - 226 - 84 PLCC
  - 236 - 100 PQFP

\* FAS216 will refer to FAS226 and FAS236 except as noted

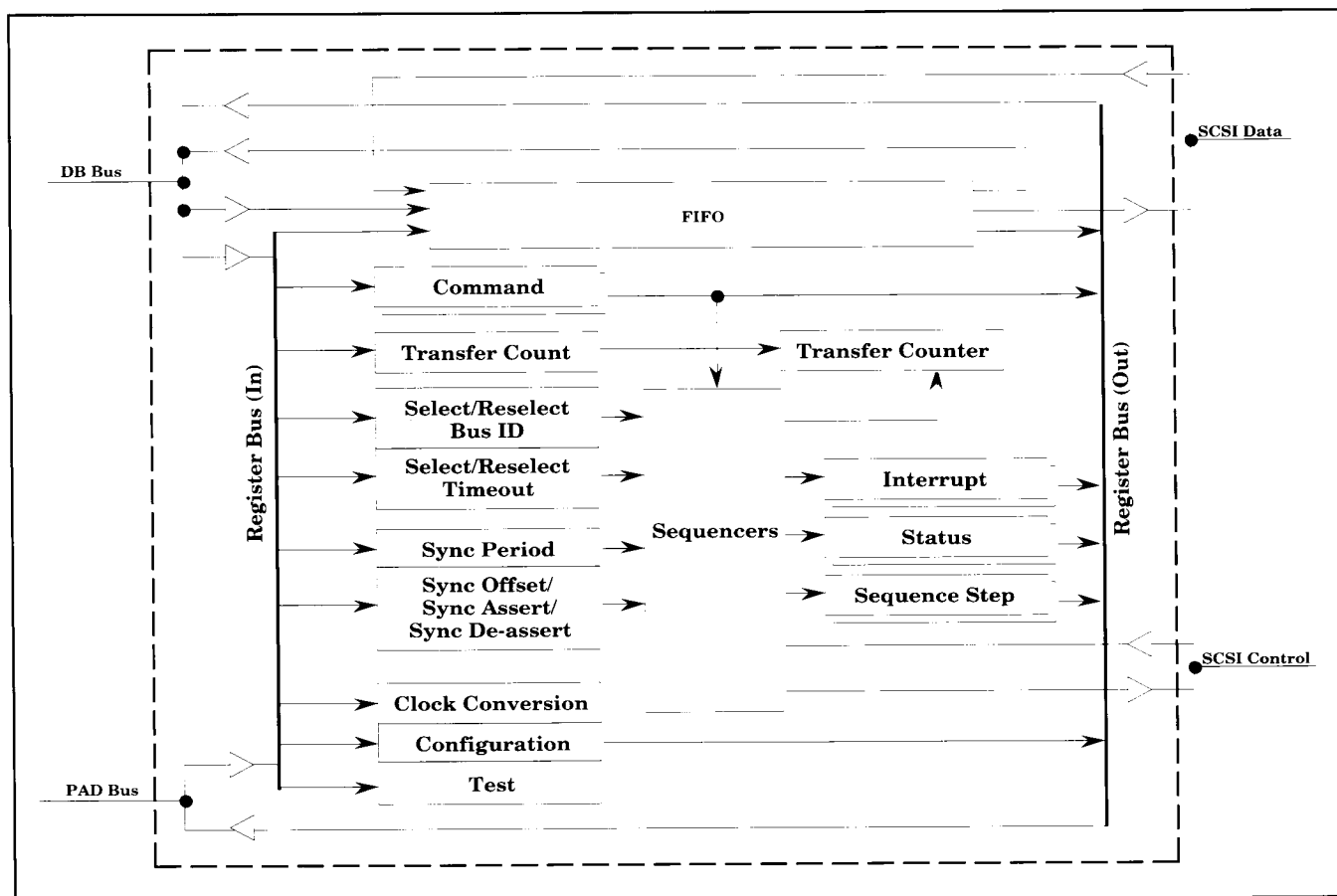


Figure 1. FAS216 Block Diagram  
Mode 2/3

## PRODUCT DESCRIPTION

The FAS216, FAS226, and FAS236 are new additions to the Emulex SCSI Processor (ESP) chip family with features designed to facilitate SCSI-2 support. The major new feature of the FAS chip is its ability to transfer synchronous data at 10 Mbytes per second. The current 5 Mbytes per second transfer rate is also supported on-chip by setting a register. Asynchronous transfers up to 7 Mbytes per second are supported as well.

Of the three versions of the chip, the FAS216 supports single-ended operations; the FAS226 supports differential only; and the FAS236 supports both single-ended and differential operations. Since the FAS216 operates in both the Initiator and Target roles, it can be used in both host and peripheral applications. The chip performs such functions as bus arbitration, selection of a target, or reselection of an initiator. The FAS216 also handles message, command, status, and data transfers between the SCSI Bus and its internal FIFO or a buffer memory.

The chip maximizes protocol efficiency by utilizing a first-in, first-out command pipeline and combination commands to minimize host intervention. The FAS216 also maximizes transfer rates by sustaining asynchronous data rates up to 7 MB/sec and, in the FAST SCSI mode, synchronous data rates up to 10 MB/sec.

The FAS216 controller systems support three main busses: the 8-bit SCSI Bus, the 8-bit or 16-bit Data Bus (DB), and the 8-bit Processor Address (PAD) bus. This versatile split-bus architecture separates the two high traffic information flows of the system, providing maximum efficiency and throughput. Figure 1 shows the internal architecture of the FAS216.

The FAS216 replaces existing SCSI interface circuitry which typically consists of discrete devices, external drivers, and a low performance SCSI interface chip. It contains a fast DMA interface, a 16-byte FIFO, and fast asynchronous and synchronous data interfaces to the SCSI Bus, including drivers.

The FAS216 has been optimized for interaction with the controller processor. Common SCSI bus sequences that would typically require significant amounts of time have been reduced to single commands. The commands are:

| Sequence                   | Description                                                                                                                                        |
|----------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------|
| Selection                  | Arbitration, target selection, transmission of optional 1- or 3-byte message followed by multiple-byte command                                     |
| Reselection                | Arbitration, initiator reselection, and transmission of a 1-byte message                                                                           |
| Bus-initiated Selection    | Transmission of selection bus ID, a 1-byte Identify or null message, a 2-byte Queue Tag Message (if SCSI-2 mode), followed by Command Phase bytes. |
| Bus-initiated Reselection  | Reselection detection and receipt of a 1-byte message.                                                                                             |
| Target Command Complete    | Transmission of a status byte and a 1-byte message.                                                                                                |
| Target Disconnect Sequence | Transmission of two 1-byte messages followed by disconnection from the SCSI bus                                                                    |
| Initiator Command Complete | Receipt of a status byte and a 1-byte message                                                                                                      |

## SYSTEM ORGANIZATION

The FAS216 chip provides the host with a complete SCSI interface. An 8-bit microprocessor bus (PAD) provides access to all internal registers and an 18-bit DMA bus (DB) provides a path for DMA transfers through the FIFO.

The versatile architecture supports various microprocessor and DMA bus configurations such as the following:

- ❑ Microprocessor interface via the PAD bus or the DB bus
- ❑ PAD bus selectable as data-only bus or as a multiplexed address and data bus
- ❑ DB bus selectable for 8-bit transfers, 16-bit transfers with byte control

FAS216 bus configuration is selected by pulling the MODE1 and MODE0 signals up or down, as shown in Table 1.

| Mode No. | Mode |   | Register |         | Register                                   |
|----------|------|---|----------|---------|--------------------------------------------|
|          | 1    | 0 | Addr     | Data    |                                            |
| 0        | 0    | 0 | A3-0     | DB Bus  | Single-bus, 8-bit DMA                      |
| 1        | 0    | 1 | A3-0     | DB Bus  | Single-bus, 16-bit DMA                     |
| 2        | 1    | 0 | PAD3-0   | PAD Bus | Split-bus, 16-bit DMA, byte control option |
| 3        | 1    | 1 | PAD3-0   | PAD Bus | Split-bus, 16-bit DMA                      |

**Table 1. Bus Configuration**

## PROCESSOR INTERFACE

The processor can interface to the FAS216 using either the PAD bus or the DB bus. Both interfaces allow the processor to read and write to all chip registers, including the FIFO. The PAD bus allows the processor interface to the chip registers independent of DMA activity on the DB bus. All register accesses are 8-bits wide.

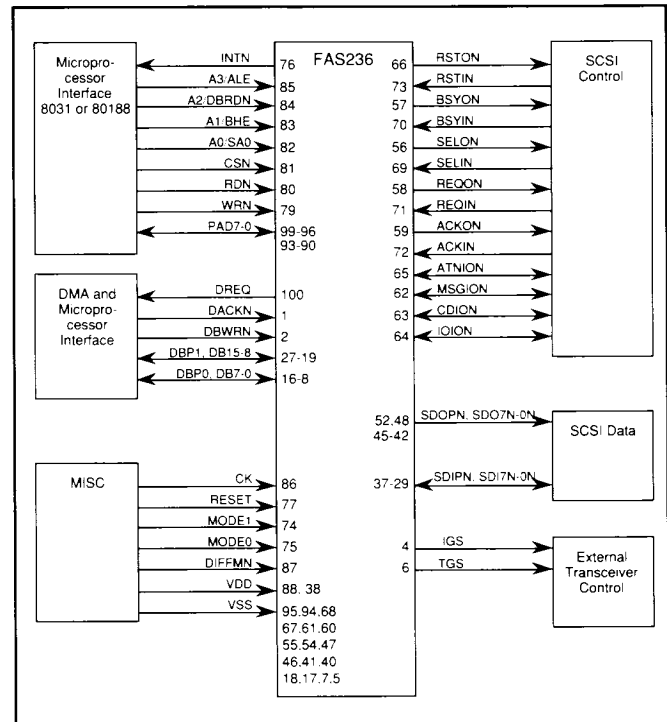
## DMA INTERFACE

The FAS216 DMA logic transfers data to and from a buffer over the DB bus, which may be configured as either 8-bit or 16-bit.\* If byte control mode is enabled, an external DMA controller can control how the bytes are placed on the bus.

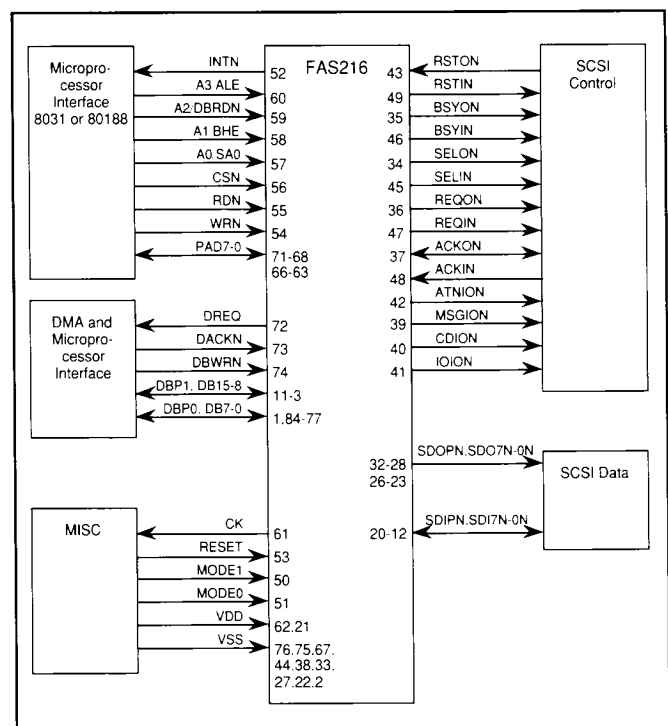
\* Each byte on the bus has its own parity.

## SIGNALS

The FAS216 acts as the interface between the microprocessor and the SCSI Bus, in either the target or initiator mode. Refer to Figure 2 (FAS216/226 Functional Signal Grouping) and Figure 3 (FAS236 Functional Signal Grouping) which show which pins interface with the microprocessor and which interface with the SCSI Bus.



**Figure 2. FAS236  
Functional Signal Grouping**



**Figure 3. FAS216/226  
Functional Signal Grouping**

## PACKAGING

The FAS216 and FAS226 chips are available in an 84-pin PLCC for surface or socket mounting. The FAS236 is available in a 100-pin plastic quad flat pack (PQFP).

## PIN DESCRIPTION

Figure 4 shows the signal names with each pin of the FAS216/226 84-pin PLCC. The diagram is viewed from the top of the chip, with the pins facing away from the reader. The pins for the FAS216 and 226 are identical, with the exception of pins 75 and 76. Pins

75 and 76 in FAS216 are VSS; in the FAS226, pin 75 is IGS and pin 76 is TGS.

Figure 5 shows the signal name associated with each pin of the FAS236 100-pin PQFP. The diagram is viewed from the top of the chip, with the pins facing away from the reader.

## REGISTERS

The FAS216 registers are used by the microprocessor to control the operation of the SCSI bus. Through these registers, the microprocessor can configure, command, monitor, and pass through the chip to the SCSI bus. These registers are listed in Table 2.

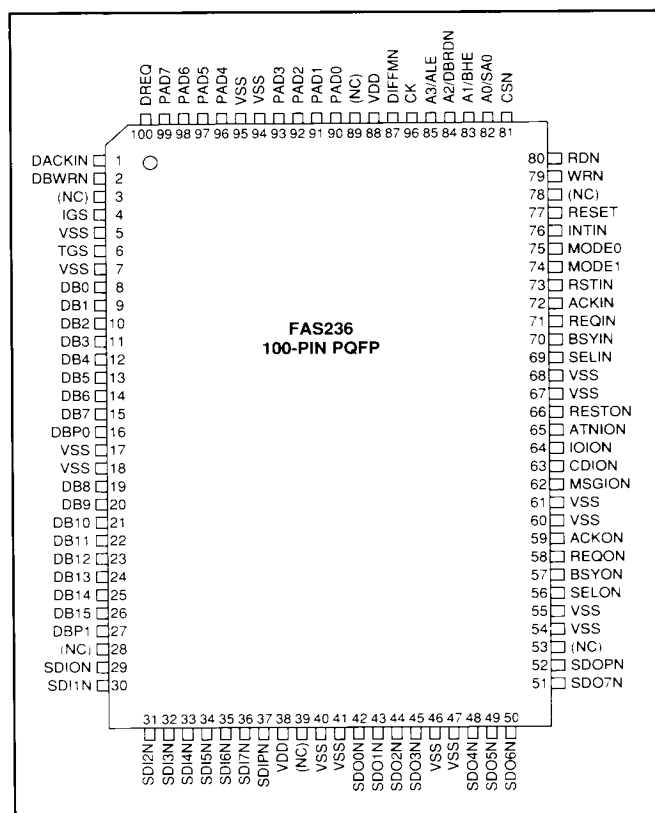
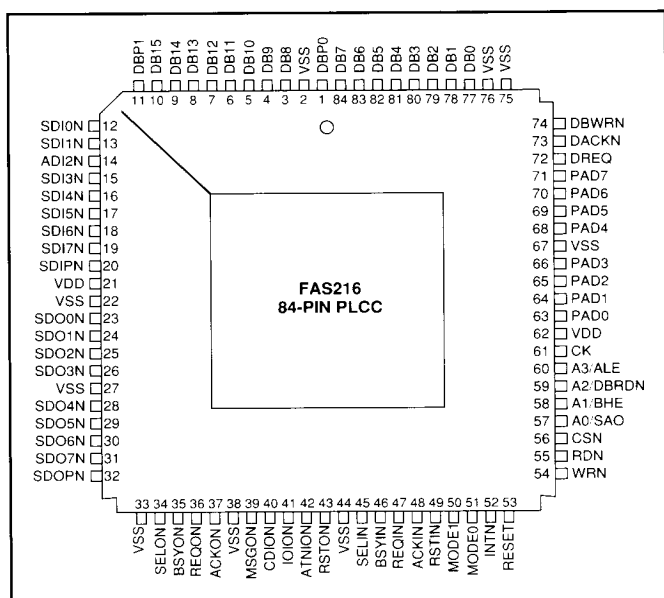
## FAS216 FEATURES/BENEFITS

### Features:

- ☐ Low SCSI Bus overhead
- ☐ Fast synchronous SCSI data transfers (10 MB/sec)
- ☐ SCSI-2 command support
- ☐ SCSI-2 feature selectability
- ☐ Parity pass-through
- ☐ Separate microprocessor and DMA busses
- ☐ 16-bit DMA Channel

### Benefits:

- ☐ Allows sharing of the SCSI Bus with more peripherals, more efficient bus utilization, fast delivery of information to host
- ☐ Can transfer data twice as fast as normal SCSI
- ☐ Allows the option of utilizing new SCSI commands
- ☐ Backward-compatible with existing chips, so SCSI-2 features can be selected when necessary
- ☐ Maintains data integrity all the way through the chip directly into the buffer
- ☐ During data transfer, the microprocessor has instant access to status and has the ability to execute commands
- ☐ High-speed information flow can be handled with the split-bus architecture to provide maximum efficiency and throughput



### Figure 5. FAS236 100-Pin PQFP Designations

| <b>FAS216<br/>Address<br/>(BFxx or<br/>FExx)</b> | <b>Register Name</b>    | <b>Type</b> | <b>FAS216<br/>Address<br/>(BFxx or<br/>FExx)</b> | <b>Register Name</b>  | <b>Type</b> |
|--------------------------------------------------|-------------------------|-------------|--------------------------------------------------|-----------------------|-------------|
| 00                                               | Transfer Counter Low    | R           | 07                                               | FIFO Flags            | R           |
|                                                  | Transfer Count Low      | W           |                                                  | Synchronous Offset    | W           |
| 01                                               | Transfer Counter Mid    | R           | 08                                               | Configuration #1      | R/W         |
|                                                  | Transfer Count Mid      | W           | 09                                               | Clock Conversion      | W           |
| 02                                               | FIFO                    | R/W         |                                                  | Factor                |             |
| 03                                               | Command                 | R/W         | 0A                                               | Test                  | W           |
| 04                                               | Status                  | R           | 0B                                               | Configuration #2      | R/W         |
|                                                  | Select/Reselect Bus ID  | W           | 0C                                               | Configuration #3      | R/W         |
| 05                                               | Interrupt               | R           | 0E                                               | Transfer Counter High | R           |
|                                                  | Select/Reselect Timeout | W           |                                                  | Transfer Count High   | W           |
| 06                                               | Sequence Step           | R           | 0F                                               | FIFO Bottom           | W           |
|                                                  | Synch Transfer Period   | W           |                                                  |                       |             |

### Table 2. FAS216 Registers

## AC TIMING

The following figures and table values that accompany them are illustrative of the FAS216 chip timing characteristics. For more information, see the *FAS216/226/236 Technical Manual*, VLSI51007-00.

### Register Interface Timing (In ns)

| # | Symbol             | Description           | Min | Max | Note |
|---|--------------------|-----------------------|-----|-----|------|
| 1 | <sup>T</sup> RASC  | Address Setup to CSN  | 0   |     | 1    |
| 2 | <sup>T</sup> RAHC  | Address Hold from CSN | 30  |     | 1    |
| 3 | <sup>T</sup> RALSA | Address Setup to ALE  | 10  |     | 2    |
| 4 | <sup>T</sup> RALHA | Address Hold from ALE | 10  |     | 2    |
| 5 | <sup>T</sup> RALD  | ALE Pulse Width       | 20  |     | 2    |
| 6 | <sup>T</sup> RALSC | ALE to CSN            | 10  |     | 2    |
| 7 | <sup>T</sup> RALHC | ALE from CSN          | 50  |     | 2    |
| 8 | <sup>T</sup> RCCY  | CSN High to CSN Low   | 30  |     |      |

### Read Cycle

| #  | Symbol             | Description              | Min | Max | Note |
|----|--------------------|--------------------------|-----|-----|------|
| 9  | <sup>T</sup> RCSR  | CSN Low to RDN Low       | 0   |     |      |
| 10 | <sup>T</sup> RRD   | RDN Pulse Width          | 30  |     |      |
| 11 | <sup>T</sup> RCHR1 | RDN High to CSN High     | 0   |     |      |
| 12 | <sup>T</sup> RCHR2 | RDN High to CSN Low      | 40  |     |      |
| 13 | <sup>T</sup> TRDC  | CNS Low to Data          |     | 65  | 3    |
| 14 | <sup>T</sup> TRDR  | RDN Low to Data          |     | 30  | 3    |
| 15 | <sup>T</sup> TRDHC | CSN High to Data Release | 2   | 30  | 4    |
| 16 | <sup>T</sup> TRDHR | RDN High to Data Release | 2   | 30  | 4    |

### Write Cycle

| #  | Symbol             | Description             | Min | Max | Note |
|----|--------------------|-------------------------|-----|-----|------|
| 17 | <sup>T</sup> CSW   | CSN Low to WRN Low      | 0   |     | 5,6  |
| 18 | <sup>T</sup> RWR   | WRN Pulse Width         | 30  |     | 6    |
| 19 | <sup>T</sup> RCHW  | WRN High to CSN High    | 0   |     | 5,6  |
| 20 | <sup>T</sup> RWH   | WRN High to CSN Low     | 30  |     | 6    |
| 21 | <sup>T</sup> RWCY  | WRN High to WRN Low     | 40  |     | 6    |
| 22 | <sup>T</sup> RAHW  | WRN High to ALE         | 50  |     | 2,6  |
| 23 | <sup>T</sup> RDW   | Data Setup to WRN High  | 15  |     | 6,7  |
| 24 | <sup>T</sup> RDHW  | Data Hold from WRN High | 0   |     | 6,8  |
| 25 | <sup>T</sup> RDWC  | Data Setup to CSN High  | 10  |     | 7    |
| 26 | <sup>T</sup> RDHWC | Data Hold from CSN High | 30  |     | 8    |

Notes:

1. Bus Configuration modes #0, #1, and #3 only.
2. Bus configuration mode #2 only (multiplexed address and data mode).
3. Both <sup>T</sup>TRDC and <sup>T</sup>TRDR specifications must be met.
4. RDN edges may precede or follow CSN edges.
5. WRN edges may precede or follow CSN edges.
6. In Bus Configuration modes #0 and #1, WRN must be tied to DBWRN.
7. Either <sup>T</sup>TRDW or <sup>T</sup>TRDWC specification must met.
8. Either <sup>T</sup>TRDHW or <sup>T</sup>TRDHWC specification must met.

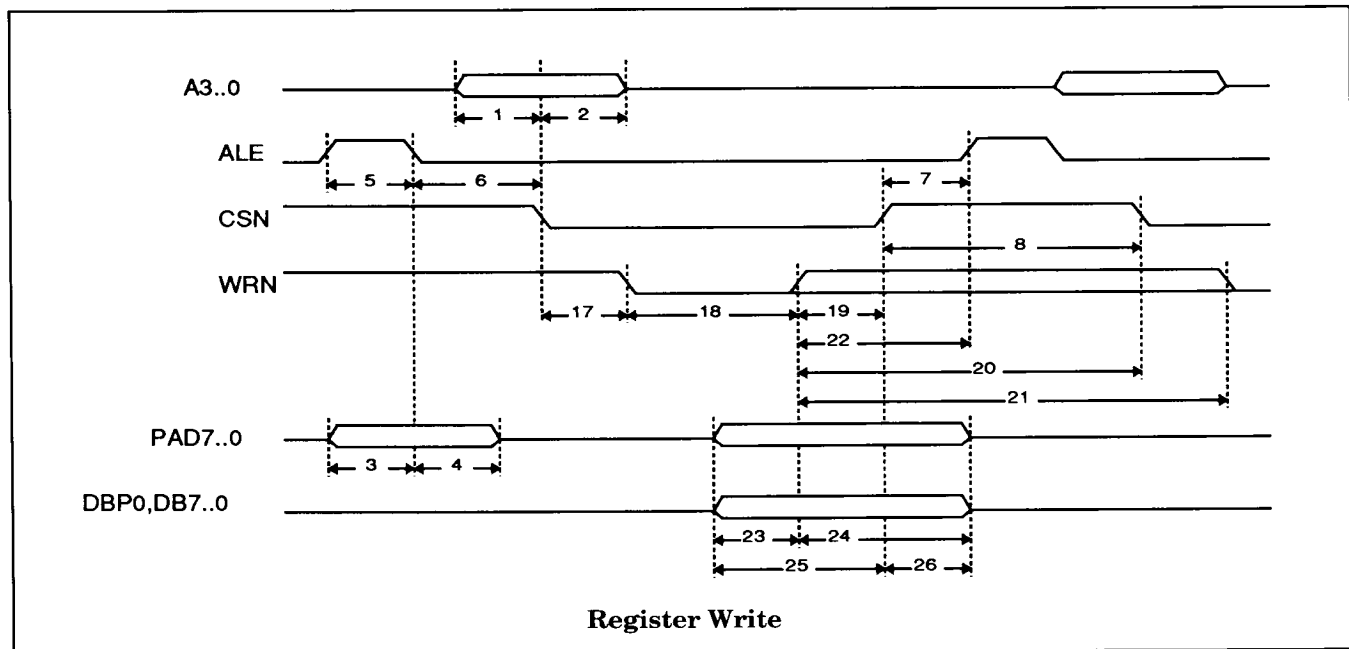
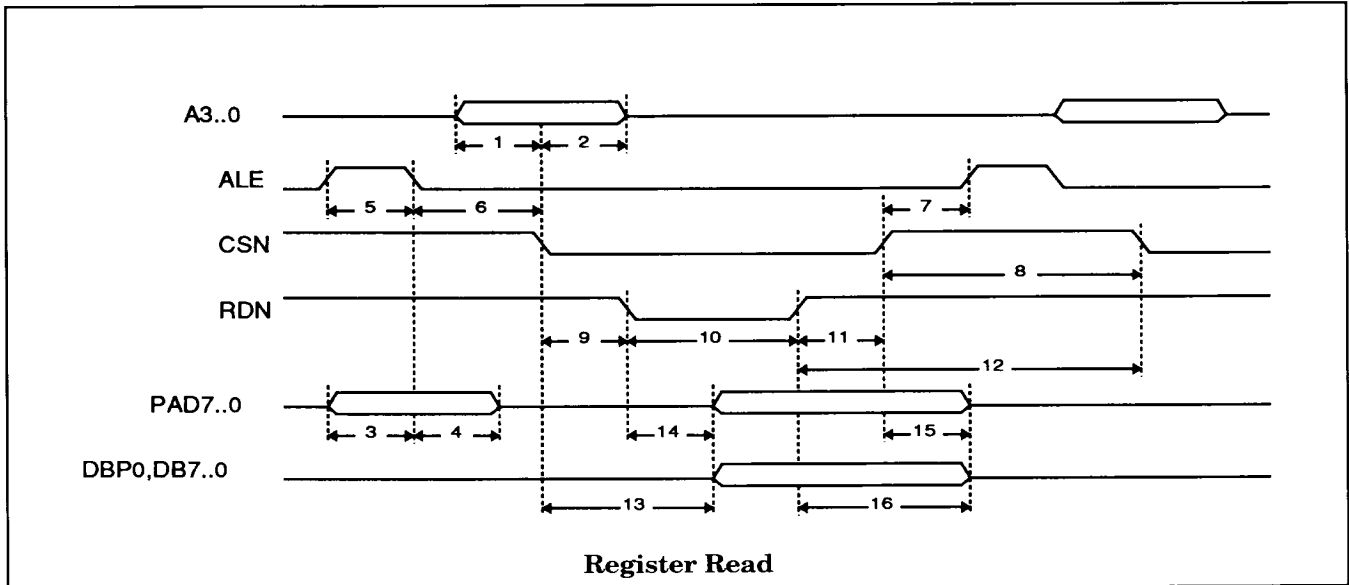


Figure 6. Register Access

## DMA Interface Timing (In ns)

| # | Symbol     | Description              | Min           | Max | Note |
|---|------------|--------------------------|---------------|-----|------|
| 1 | $T_{DARL}$ | DACKN Low to DREQ Low    |               | 30  | 1    |
| 2 | $T_{DRH}$  | DACKN High to DREQ High  |               | 30  | 2    |
| 3 | $T_{DACY}$ | DACKN High to DACKN Low  | 12            |     |      |
| 4 | $T_{ACK}$  | DACKN Pulse Width        | 45            |     |      |
| 5 | $T_{ACP0}$ | DACKN Low to DACKN Low   | 95            |     |      |
| 6 | $T_{ACP1}$ | DACKN High to DACKN High | $T_{CS} + 25$ |     | 12   |

### Read Cycle

| #  | Symbol      | Description                  | Min | Max | Note |
|----|-------------|------------------------------|-----|-----|------|
| 7  | $T_{DBSSR}$ | BHE/SA0 Setup to DBRDN Low   | 20  |     | 3,4  |
| 8  | $T_{DBSHR}$ | BHE/SA0 Hold from DBRDN High | 20  |     | 3,4  |
| 9  | $T_{DAR}$   | DACKN Low to DBRDN Low       | 0   |     | 3,6  |
| 10 | $T_{DRD}$   | DBRDN Pulse Width            | 35  |     | 3    |
| 11 | $T_{DRA}$   | DBRDN High to DACKN High     | 0   |     | 3,7  |
| 12 | $T_{DDAH}$  | DACKN High to Data           | 45  |     | 5    |
| 13 | $T_{DDAL}$  | DACKN Low to Data            | 30  |     | 5    |
| 14 | $T_{DDRL}$  | DBRDN Low to Data            | 35  |     | 3,5  |
| 15 | $T_{DADR}$  | DACKN High to Data Release   | 2   | 25  |      |
| 16 | $T_{DRDR}$  | DBRDN High to Data Release   | 2   | 35  | 3    |

### Write Cycle

| #  | Symbol      | Description                  | Min | Max | Note |
|----|-------------|------------------------------|-----|-----|------|
| 17 | $T_{DBSSW}$ | BHE/SA0 Setup to DBWRN Low   | 20  |     | 3,4  |
| 18 | $T_{DBSHW}$ | BHE/SA0 Hold from DBWRN High | 20  |     | 3,4  |
| 19 | $T_{DAW}$   | DACKN Low to DBWRN Low       | 0   |     | 8    |
| 20 | $T_{DWR}$   | DBWRN Pulse Width            | 30  |     |      |
| 21 | $T_{DWA}$   | DBWRN High to DACKN High     | 0   |     | 9    |
| 22 | $T_{DWCY}$  | DBWRN High to DBWRN Low      | 25  |     |      |
| 23 | $T_{DDW}$   | Data Setup to DBWRN High     | 15  |     | 10   |
| 24 | $T_{DHW}$   | Data Hold from DBWRN High    | 0   |     | 11   |
| 25 | $T_{DDWA}$  | Data Setup to DACKN High     | 10  |     | 10   |
| 26 | $T_{DHWA}$  | Data Hold from DACKN High    | 10  |     | 11   |

#### Notes:

1. Negation pending.
2. Assertion pending.
3. Bus configuration mode #2 only.
4. Byte control mode only.
5.  $T_{DDAH}$  and  $T_{DDAL}$  specifications must be met.
6. DBRDN low may precede DACKN low.
7. DBRDN low may follow DACKN high.
8. DBWRN low may precede DACKN low.
9. DBWRN low may follow DACKN high.
10. Either  $T_{DDW}$  or  $T_{DDWA}$  specification must be met.
11. Either  $T_{DHW}$  or  $T_{DHWA}$  specification must be met.
12. Synchronous transfers only.

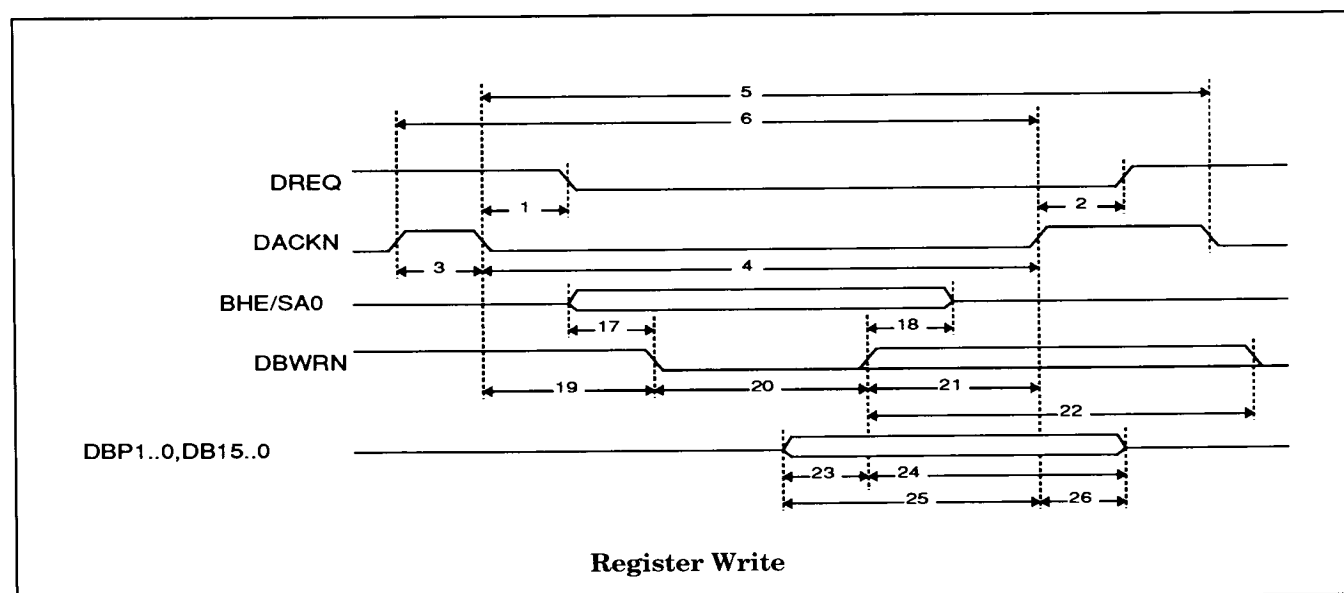
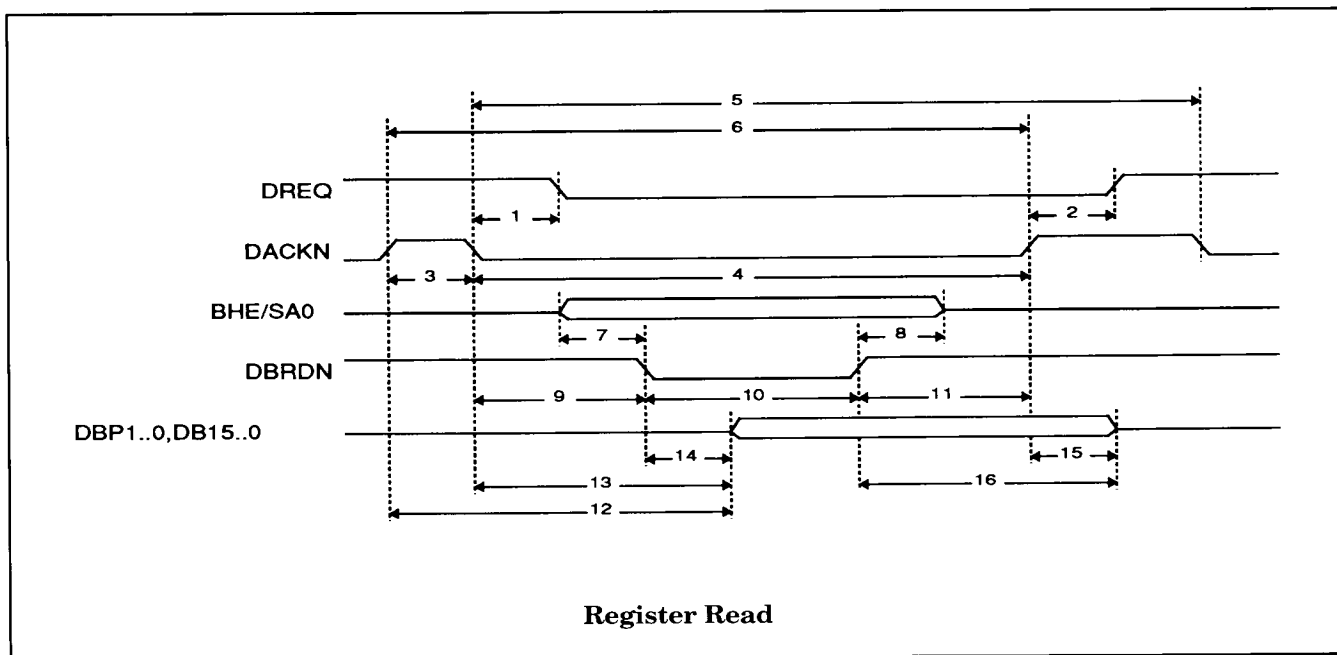


Figure 7. DMA Access

### Alternate DMA Interface Timing (In ns)

| # | Symbol            | Description               | Min | Max | Note |
|---|-------------------|---------------------------|-----|-----|------|
| 1 | <sup>T</sup> DARL | DAACKN Low to DREQ Low    |     | 30  | 1,10 |
| 2 | <sup>T</sup> DRH  | DAACKN High to DREQ High  |     | 30  | 2    |
| 3 | <sup>T</sup> DACY | DAACKN High to DAACKN Low | 60  |     |      |
| 4 | <sup>T</sup> ACK  | DAACKN Pulse Width        | 70  |     |      |

#### Read Cycle

| #  | Symbol             | Description                      | Min | Max | Note    |
|----|--------------------|----------------------------------|-----|-----|---------|
| 5  | <sup>T</sup> DBSSR | BHE/SA0 Setup to RDN/DBRDN Low   | 20  |     | 3,4     |
| 6  | <sup>T</sup> DBSHR | BHE/SA0 Hold from RDN/DBRDN High | 20  |     | 3,4     |
| 7  | <sup>T</sup> DAR   | DAACKN Low to RDN/DBRDN Low      | 0   |     | 6,12    |
| 8  | <sup>T</sup> DRD   | RDN/DBRDN Pulse Width            | 70  |     | 12      |
| 9  | <sup>T</sup> DRA   | RDN/DBRDN High to DAACKN High    | 0   |     | 7,12    |
| 10 | <sup>T</sup> DRRL  | RDN/DBRDN High to DREQ Low       | 90  |     | 1,11,12 |
| 11 | <sup>T</sup> DRACY | RDN/DBRDN High to RDN/DBRDN Low  | 60  |     | 11, 12  |
| 12 | <sup>T</sup> DDAH  | DAACKN High to Data              | 45  |     | 5       |
| 13 | <sup>T</sup> DDAL  | DAACKN Low to Data               | 35  |     | 5       |
| 14 | <sup>T</sup> DDRL  | RDN/DBRDN Low to Data            | 55  |     | 5,12    |
| 15 | <sup>T</sup> DADR  | DAACKN High to Data Release      |     | 25  |         |
| 16 | <sup>T</sup> DRDR  | RDN/DBRDN High to Data Release   |     | 45  | 12      |

#### Write Cycle

| #  | Symbol             | Description                  | Min | Max | Note |
|----|--------------------|------------------------------|-----|-----|------|
| 17 | <sup>T</sup> DBSSW | BHE/SA0 Setup to DBWRN Low   | 20  |     | 3,4  |
| 18 | <sup>T</sup> DBSHW | BHE/SA0 Hold from DBWRN High | 20  |     | 3,4  |
| 19 | <sup>T</sup> DAW   | DAACKN Low to DBWRN Low      | 0   |     | 8    |
| 20 | <sup>T</sup> DWR   | DBWRN Pulse Width            | 70  |     |      |
| 21 | <sup>T</sup> DWA   | DBWRN High to DAACKN High    | 0   |     | 9    |
| 22 | <sup>T</sup> DWRL  | DBWRN High to DREQ Low       | 90  |     | 11   |
| 23 | <sup>T</sup> DWCY  | DBWRN High to DBWRN Low      | 60  |     | 11   |
| 24 | <sup>T</sup> DDW   | Data Setup to DBWRN High     | 15  |     |      |
| 25 | <sup>T</sup> DHW   | Data Hold from DBWRN High    | 0   |     |      |

Notes:

1. Negation pending.
2. Assertion pending.
3. Bus configuration mode #2 only.
4. Byte control mode only.
5. <sup>T</sup>DDAH and <sup>T</sup>DDAL specifications must be met.
6. RDN/DBRDN low may precede DAACKN low.
7. RDN/DBRDN high may follow DAACKN high.
8. DBWRN low may precede DAACKN low.
9. DBWRN high may follow DAACKN high.
10. Single DMA transfers only.
11. Multiple DMA transfers only.
12. The DMA Read line is defined as RDN in Bus Configuration Modes #0 and #1, and as DBRDN in Bus Configuration Mode #2. In Bus Configuration Mode #3 there is no DMA read line, and DAACKN must toggle for each DMA read cycle.

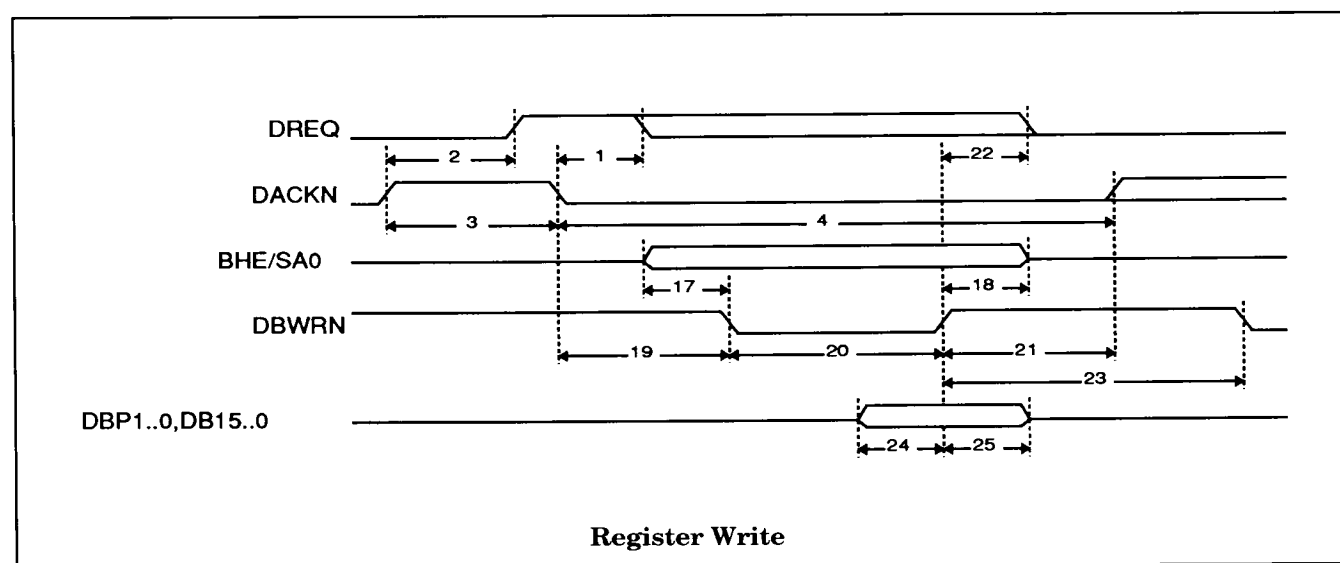
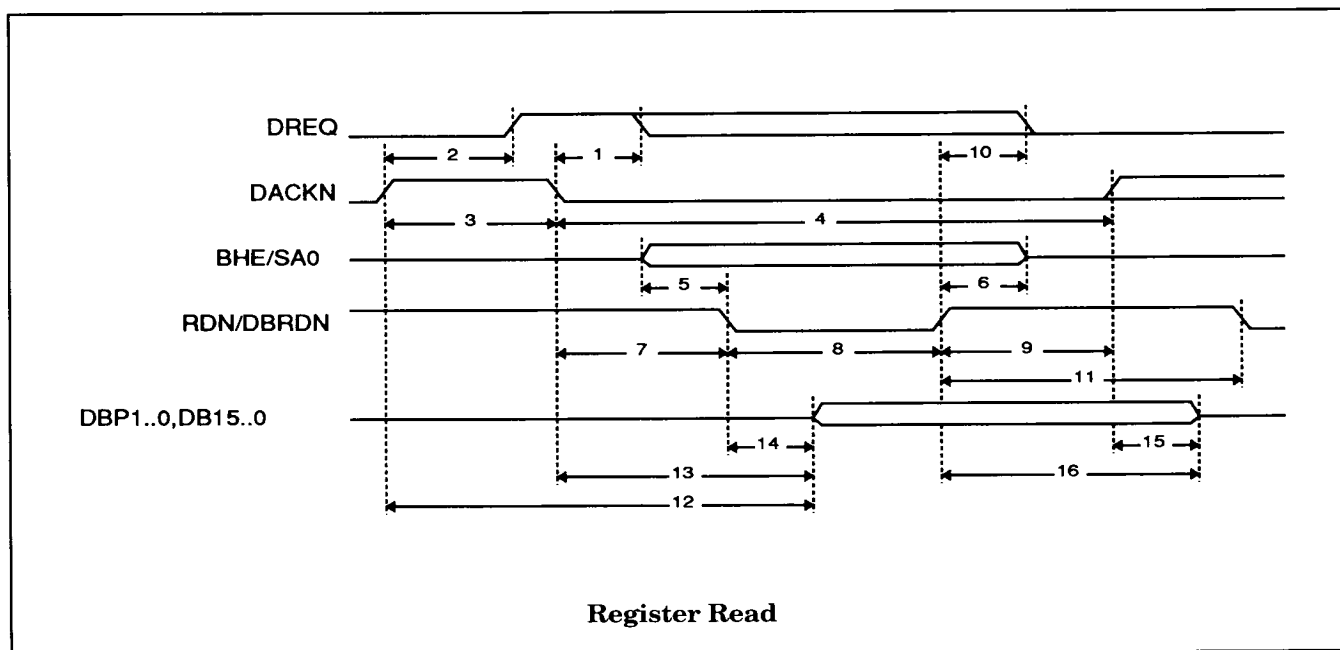


Figure 8. Alternate DMA Access

## SCSI Asynchronous Timing

### SINGLE-ENDED MODE<sup>1</sup>

| # | Symbol             | Description              | Min | Max | Note |
|---|--------------------|--------------------------|-----|-----|------|
| 1 | <sup>T</sup> AAR01 | ACKIN Low to REQON High  |     | 50  |      |
| 2 | <sup>T</sup> AAR02 | ACKIN High to REQON Low  |     | 45  | 3,6  |
| 3 | <sup>T</sup> ARA01 | REQIN High to ACKON High |     | 50  |      |
| 4 | <sup>T</sup> ARA02 | REQIN Low To ACKON Low   |     | 50  | 4,6  |

#### Output Cycle

| # | Symbol             | Description               | Min | Max | Note |
|---|--------------------|---------------------------|-----|-----|------|
| 5 | <sup>T</sup> ARDSO | Data Setup to REQON Low   | 60  |     |      |
| 5 | <sup>T</sup> AADSO | Data Setup to ACKON Low   | 60  |     |      |
| 6 | <sup>T</sup> ARHDO | Data Hold from REQIN High | 5   |     | 5    |
| 6 | <sup>T</sup> AAHDO | Data Hold from ACKIN Low  | 5   |     | 5    |

### DIFFERENTIAL MODE<sup>2</sup>

| # | Symbol             | Description              | Min | Max | Note |
|---|--------------------|--------------------------|-----|-----|------|
| 1 | <sup>T</sup> AAR01 | ACKIN Low to REQON High  |     | 30  |      |
| 2 | <sup>T</sup> AAR02 | ACKIN High to REQON Low  |     | 30  | 3,6  |
| 3 | <sup>T</sup> ARA01 | REQIN High to ACKON High |     | 25  |      |
| 4 | <sup>T</sup> ARA02 | REQIN Low to ACKON Low   |     | 30  | 4,6  |

#### Output Cycle

| # | Symbol             | Description               | Min | Max | Note |
|---|--------------------|---------------------------|-----|-----|------|
| 5 | <sup>T</sup> ARDSO | Data Setup to REQON Low   | 70  |     |      |
| 5 | <sup>T</sup> AADSO | Data Setup to ACKON Low   | 70  |     |      |
| 6 | <sup>T</sup> ARHDO | Data Hold from REQIN High | 5   |     | 5    |
| 6 | <sup>T</sup> AAHDO | Data Hold from ACKIN Low  | 5   |     | 5    |

#### Input Cycle

| # | Symbol             | Description              | Min | Max | Note |
|---|--------------------|--------------------------|-----|-----|------|
| 7 | <sup>T</sup> ARDSI | Data Setup to REQIN Low  | 0   |     |      |
| 7 | <sup>T</sup> AADSI | Data Setup to ACKIN Low  | 0   |     |      |
| 8 | <sup>T</sup> ARHDI | Data Hold from REQIN Low |     | 18  |      |
| 8 | <sup>T</sup> AAHDI | Data Hold from ACKIN Low |     | 18  |      |

#### Notes:

- 200pF loading, data out on lines SDOPN, SDO7N-0N.
- Data out on lines SDIPN, SDI7N-0N.
- <sup>T</sup>ARDSO specification must also be met (output cycle only).
- <sup>T</sup>AADSO specification must also be met (output cycle only).
- FIFO is not empty.
- FIFO is not full (input cycle only).

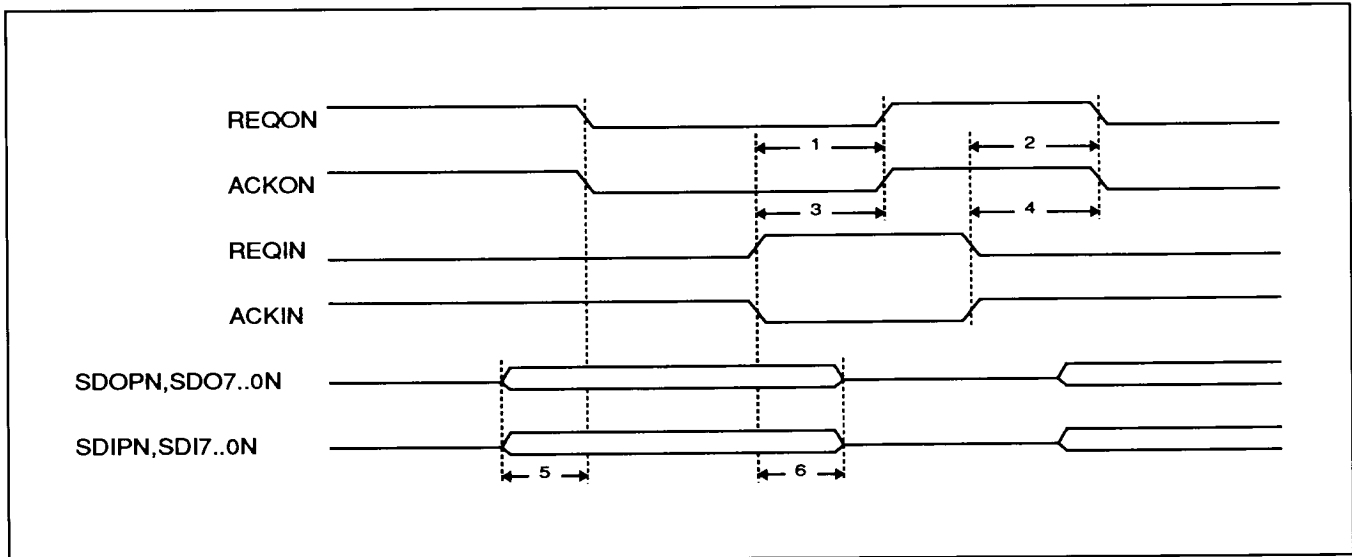


Figure 9. SCSI Asynchronous Timing

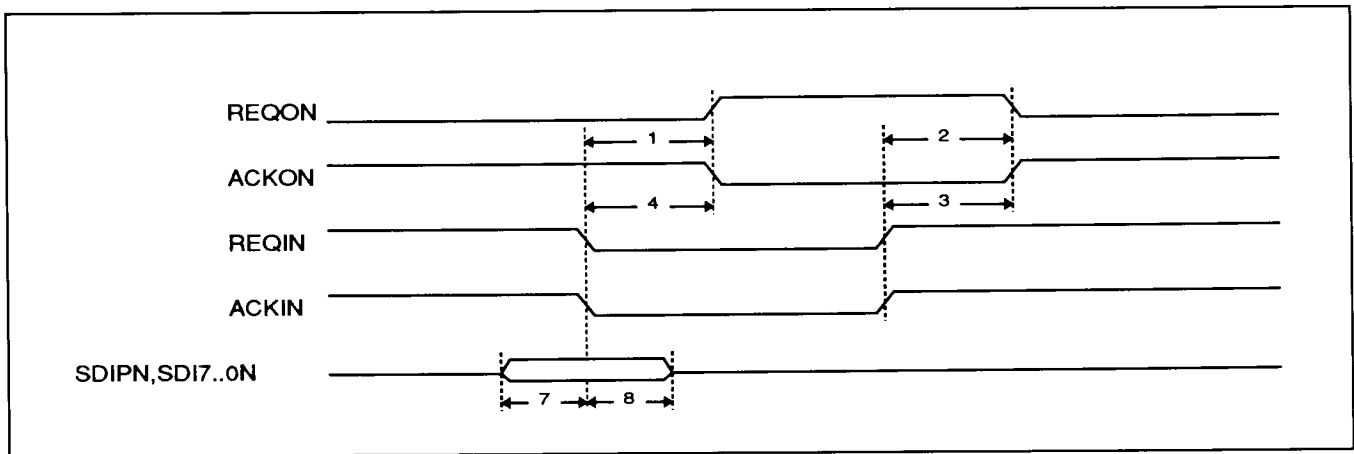


Figure 10. SCSI Asynchronous Input

# SCSI Synchronous Timing (In ns)

## OUTPUT CYCLE Normal SCSI, Single-Ended Mode<sup>1</sup>

| # | Symbol             | Description                        | Min | Max |
|---|--------------------|------------------------------------|-----|-----|
| 1 | <sup>T</sup> SASTO | REQON/ACKON Assertion Period       | 90  |     |
| 2 | <sup>T</sup> SNEGO | REQON/ACKON Negation Period        | 90  |     |
| 3 | <sup>T</sup> SDSO  | Data Setup to REQON Low/ACKON Low  | 55  |     |
| 4 | <sup>T</sup> SHDO  | Data Hold from REQON Low/ACKON Low | 100 |     |

## Normal SCSI, Differential Mode<sup>2</sup>

| # | Symbol             | Description                        | Min | Max |
|---|--------------------|------------------------------------|-----|-----|
| 1 | <sup>T</sup> SASTO | REQON/ACKON Assertion Period       | 96  |     |
| 2 | <sup>T</sup> SNEGO | REQON/ACKON Negation Period        | 96  |     |
| 3 | <sup>T</sup> SDSO  | Data Setup to REQON Low/ACKON Low  | 65  |     |
| 4 | <sup>T</sup> SHDO  | Data Hold from REQON Low/ACKON Low | 110 |     |

## FAST SCSI, Single-Ended Mode<sup>3</sup>

| # | Symbol             | Description                        | Min | Max |
|---|--------------------|------------------------------------|-----|-----|
| 1 | <sup>T</sup> SASTO | REQON/ACKON Assertion Period       | 30  |     |
| 2 | <sup>T</sup> SNEGO | REQON/ACKON Negation Period        | 30  |     |
| 3 | <sup>T</sup> SDSO  | Data Setup to REQON Low/ACKON Low  | 25  |     |
| 4 | <sup>T</sup> SHDO  | Data Hold from REQON Low/ACKON Low | 35  |     |

## FAST SCSI, Differential Mode<sup>4</sup>

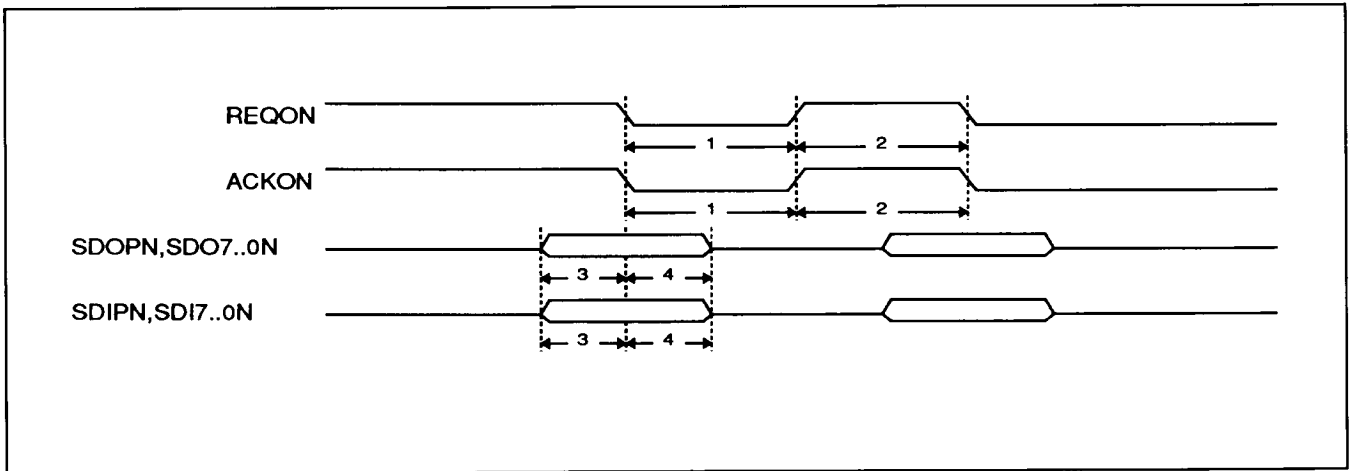
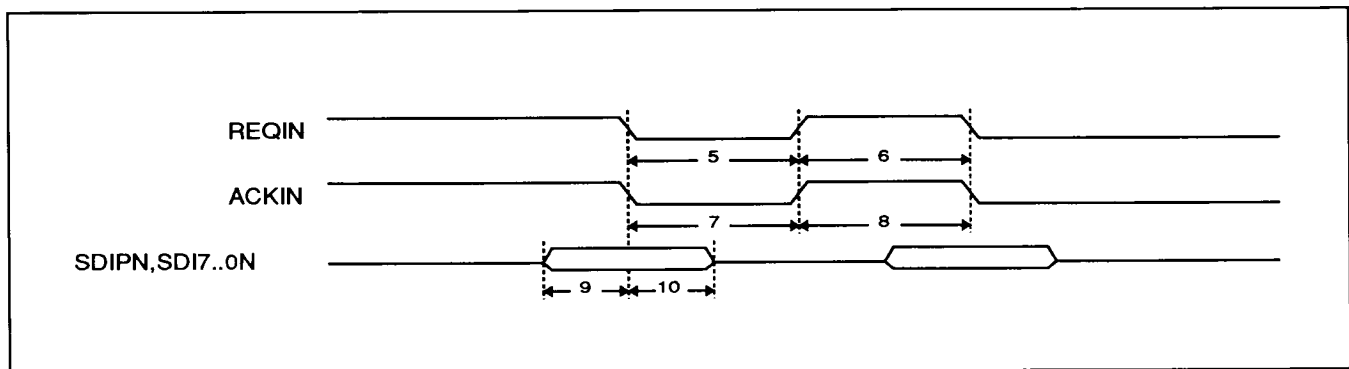
| # | Symbol             | Description                        | Min | Max |
|---|--------------------|------------------------------------|-----|-----|
| 1 | <sup>T</sup> ASTO  | REQON/ACKON Assertion Period       | 40  |     |
| 2 | <sup>T</sup> SNEGO | REQON/ACKON Negation Period        | 40  |     |
| 3 | <sup>T</sup> SDSO  | Data Setup to REQON Low/ACKON Low  | 35  |     |
| 4 | <sup>T</sup> SHDO  | Data Hold from REQON Low/ACKON Low | 45  |     |

## INPUT CYCLE

| #  | Symbol              | Description                        | Min | Max |
|----|---------------------|------------------------------------|-----|-----|
| 5  | <sup>T</sup> SRASTI | REQIN Assertion Period             | 27  |     |
| 6  | <sup>T</sup> SRNEGI | REQIN Negation Period              | 20  |     |
| 7  | <sup>T</sup> SAASTI | ACKIN Assertion Period             | 20  |     |
| 8  | <sup>T</sup> SANEGI | ACKIN Negation Period              | 20  |     |
| 9  | <sup>T</sup> SDSI   | Data Setup to REQIN Low/ACKIN Low  | 5   |     |
| 10 | <sup>T</sup> SHDI   | Data Hold from REQIN Low/ACKIN Low | 15  |     |

### Notes:

- 5MBytes/sec max., data out on lines SDOPN, SDO7N-0N
- 5MBytes/sec max., data out on lines SDIPN, SDI7N-0N
- 10MBytes/sec max., data out on lines SDOPN, SDO7N-0N
- 10MBytes/sec max., data out on lines SDIPN, SDI7N-0

**Figure 11. SCSI Synchronous Output****Figure 12. SCSI Synchronous Input**



NOTES:

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