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NCR89C100
Chip Specification

Overview

The NCR89C100 is designed for low-cost, SBus-based systems. It incorporates standard workstation I/O devices with a DMA controller in a single 160-pin PQFP package, providing cost, area, and power savings over discrete implementations.

The 89C100 provides three special purpose SBus DMA channels that are commonly used on SPARC® platforms: Ethernet, SCSI, and Parallel Port. It consists of three major logic blocks: DMA2, ENET, SCSI as well as an additional TEST block. The DMA2 block provides internal buffering for each of its three channels in the form of a cache for the ENET interface and fifos for the SCSI and Parallel Port interfaces. It also provides control/status registers for each channel, plus several SCSI/PPORT-specific support registers, and a write buffer for slave accesses to the ENET. The DMA2 block design is based on the L64853[1] ASIC design with the addition of a programmable, Centronics-type parallel port. It incorporates a number of new features for increasing performance and allowing different modes of operation necessary for future desktop systems. The ENET block is based on the NCR92C990 Application Specific Function (ASF) which is a superset of (and fully backwards compatible with) the AM7990[2] previously found on SPARCstations. The SCSI block is based on the NCR53C9X[3] ASF which is a superset of (and fully backwards compatible with) the NCR53C90A also found on SPARCstations. The TEST block contains the JTAG TAP controller, JTAG boundary scan cells, ASF test muxes and some ancillary glue logic.

The 89C100 interfaces directly to the SBus with no additional glue logic. Together, with the 89C105 (slave I/O), it provides the core SPARCstation I/O subsystem.

This document reflects the integrated nature of the 89C100. This section, "NCR89C100 Master I/O", covers the chip as a whole and describes pinout information, test muxing, chip-level block diagrams and address map, and electrical and mechanical characteristics. The TEST block is described in detail, but DMA2, ENET, and SCSI blocks are only introduced and a list of differences from their discrete implementations is given. The full specifications for those discrete implementations follow in the next three sections: "DMA2 DMA Core," "NCR92C990 Ethernet Core," and "NCR53C9X SCSI Core". These specifications cover functional descriptions and theory of operations.

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1. LSI Logic Corp.
2. Advanced Micro Devices, Inc.
3. The NCR53C9X is identical to the FAS101 licensed from Emulex Corporation.

Chip-Level Functional Block Diagram

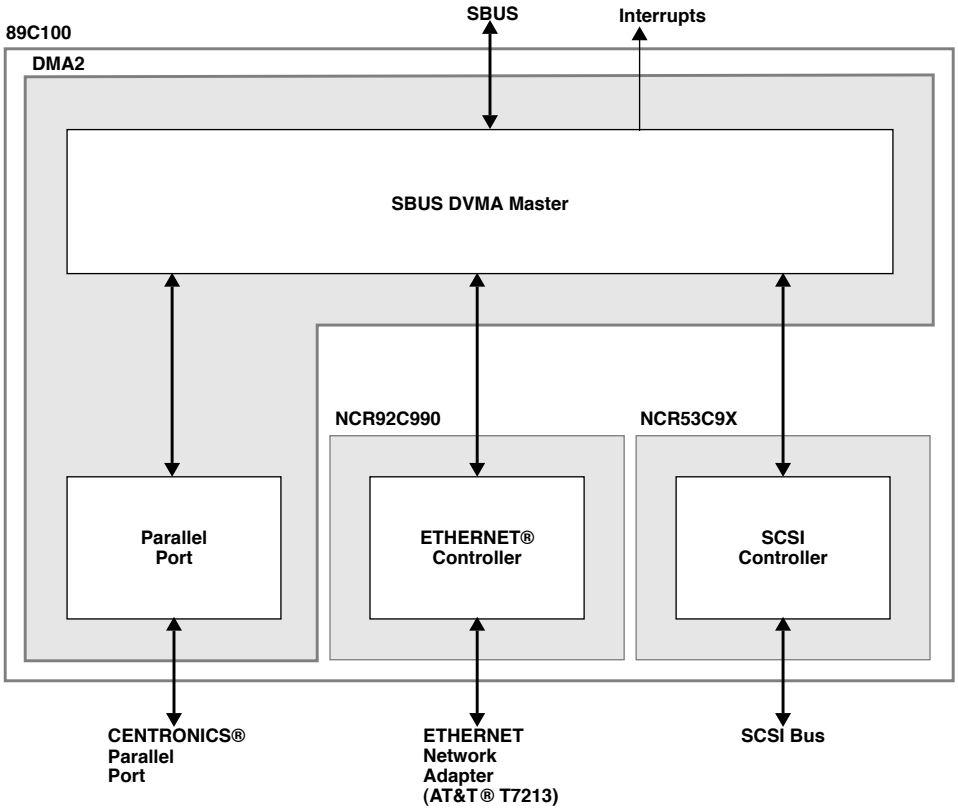


Figure 2-1 Chip-Level Functional Block Diagram

Features

- Single chip solution to standard SPARC DVMA devices - saves cost, power, board space, and weight. Together, with the 89C105 chip, forms a two-chip solution which provides the core SPARCstation I/O subsystem.
- Supports concurrent 10 MByte/sec SCSI transfers, 1.25 MByte/sec Ethernet transfers, and 4 MByte/sec Parallel Port transfers.
- Supports 4-word, 8-word, and 'no burst' SBus burst modes.
- 64-byte internal cache for Ethernet data buffering.
- 64-byte internal FIFOs for SCSI and Parallel Port data buffering.
- 16-bit write buffer for slave writes to Ethernet.
- Improved cache and FIFO draining algorithms for better SBus utilization.
- Internal address and byte count registers and"NEXT" address/byte count features for data block chaining on SCSI and Parallel Port interfaces.
- JTAG internal and boundary scan for improved chip and board level testability.

Intended Applications

The 89C100 is intended for low-end SBus-based systems in which cost, power, and area are the main design constraints. It is designed for use with either the Texas Instruments MicroSPARC or SuperSPARC processors, but will also work in any SBus-based system.

Related Products

The 89C100 is designed to share a single SBus slot with the NCR89C105.

Pinout Information

This section includes the pinout map and two tables that summarize the 89C100 pinout information in the following formats:

- Pinout by function
- Pinout by pin order on package
- JTAG boundary chain
- Pinout in TEST modes

Pinout Map

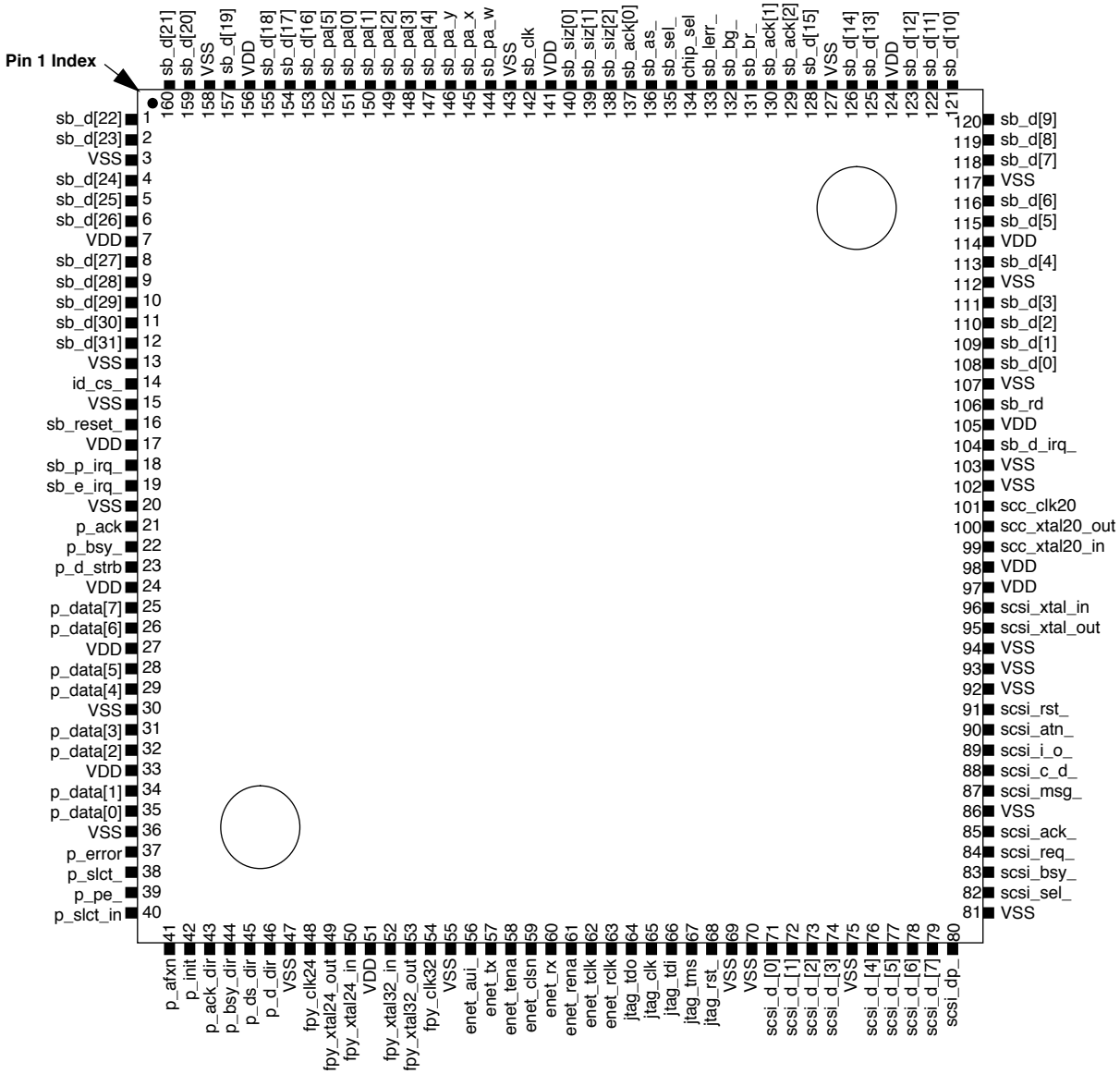


Figure 2-2 Pinout Map

Pinout Tables

Tables 2-4 and 2-5 present the 89C100 pinouts by function and by pin number sequence, respectively. The pin type entry in the Type column of Tables 2-4 and 2-5 is composed of fields which contain the mnemonic values shown in Tables 2-1 and 2-2:

Table 2-1 Valid Pin Mnemonics

Field	A	B	C	D	E	F	G	H	I
Value(s)	BS	IN	N	PD	2	L	U	25	T
	NCR	IO	—	—	4	—	D	100	H
	—	IOP			6		—	—	I
		ION			8				S16
		O			12				S18
		OT			16				S38
		IP			—				—

The values represented by the mnemonics in each of these fields is as follows:

Table 2-2 Mnemonic Descriptions

Field	Mnemonic	Description
A	BS	Boundary Scan
	NCR	NCR type
B	IN	Input
	IO	Bidirectional
	IOP	Bidirectional with pull-up/pull-down
	ION	Bidirectional open drain
	O	Output
	OT	Tristate output
	IP	Input with pull-up/pull-down
C	N	Open drain
D	PD	IO pad
E	*integer*	Pad drain in mA as indicated
F	L	Slew rate limited output
G	U	Pull-up
	D	Pull-down
H	*integer*	Pull-up/pull-down value in μA as indicated
I	T	TTL input receiver
	H	High drive TTL input receiver
	I	Inverting TTL input receiver
	S16	ds1216 Schmitt input receiver
	S18	ds1218 Schmitt input receiver
	S38	ds1238 Schmitt input receiver

For example, the pin type identification bsinpds18 means that the pin type is a boundary scan version of an input pad with a ds1218 Schmitt input receiver.

Notice that some fields in Table 2-1 are optional and that there are four exceptions to the above scheme. SCSIPAD is a 48 mA driver compatible with ANSI X3T9.2 requirements, SCSIPADF is the same with an input RC filter, OSC1401 is a crystal oscillator pad, and BSCLOCK is a clock input pad.

The Direction column in Tables 2-4 and 2-5 is used to identify the pin direction using the mnemonics shown in Table 2-3.

Table 2-3 Direction Mnemonic Descriptions

Mnemonic	Description
I	Input
O	Output
B	Bidirectional
T	Tristate
—	Not applicable

Note that the pad type listed in the following tables may not correspond exactly to the functional direction of the pin (input, output, bidirectional, or tristate) for either of the following reasons:

- The pin is used differently in a test mode. For instance, using an input as an output during test will require use of a bidirectional pad instead of an input.
- An equivalent output-only pad was not available. This applies specifically to the SBus outputs, which all use a custom 12 mA pad that was only available as a bidirectional pad.

Pinout by Function

Table 2-4 Pinout by Function

Name	Pin	Direction	Type	Description
SBus Interface: 59 pins				
sb_d[31]	12	B	BSIOPD12S16	SBus Data Bus (MSB)
sb_d[30]	11	B	BSIOPD12S16	SBus Data Bus
sb_d[29]	10	B	BSIOPD12S16	SBus Data Bus
sb_d[28]	9	B	BSIOPD12S16	SBus Data Bus
sb_d[27]	8	B	BSIOPD12S16	SBus Data Bus
sb_d[26]	6	B	BSIOPD12S16	SBus Data Bus
sb_d[25]	5	B	BSIOPD12S16	SBus Data Bus
sb_d[24]	4	B	BSIOPD12S16	SBus Data Bus
sb_d[23]	2	B	BSIOPD12S16	SBus Data Bus
sb_d[22]	1	B	BSIOPD12S16	SBus Data Bus
sb_d[21]	160	B	BSIOPD12S16	SBus Data Bus
sb_d[20]	159	B	BSIOPD12S16	SBus Data Bus
sb_d[19]	157	B	BSIOPD12S16	SBus Data Bus
sb_d[18]	155	B	BSIOPD12S16	SBus Data Bus
sb_d[17]	154	B	BSIOPD12S16	SBus Data Bus
sb_d[16]	153	B	BSIOPD12S16	SBus Data Bus
sb_d[15]	128	B	BSIOPD12S16	SBus Data Bus
sb_d[14]	126	B	BSIOPD12S16	SBus Data Bus
sb_d[13]	125	B	BSIOPD12S16	SBus Data Bus
sb_d[12]	123	B	BSIOPD12S16	SBus Data Bus
sb_d[11]	122	B	BSIOPD12S16	SBus Data Bus
sb_d[10]	121	B	BSIOPD12S16	SBus Data Bus
sb_d[9]	120	B	BSIOPD12S16	SBus Data Bus
sb_d[8]	119	B	BSIOPD12S16	SBus Data Bus
sb_d[7]	118	B	BSIOPD12S16	SBus Data Bus
sb_d[6]	116	B	BSIOPD12S16	SBus Data Bus
sb_d[5]	115	B	BSIOPD12S16	SBus Data Bus
sb_d[4]	113	B	BSIOPD12S16	SBus Data Bus
sb_d[3]	111	B	BSIOPD12S16	SBus Data Bus
sb_d[2]	110	B	BSIOPD12S16	SBus Data Bus
sb_d[1]	109	B	BSIOPD12S16	SBus Data Bus
sb_d[0]	108	B	BSIOPD12S16	SBus Data Bus (LSB)

Table 2-4 Pinout by Function (Continued)

Name	Pin	Direction	Type	Description
sb_br_	131	B	BSIOPD12T	SBus Bus Request
sb_bg_	132	I	BSINPDH	SBus Bus Grant
sb_ack[2]	129	B	BSIOPD12H	SBus Acknowledge
sb_ack[1]	130	B	BSIOPD12I	SBus Acknowledge
sb_ack[0]	137	B	BSIOPD12I	SBus Acknowledge
sb_reset_	16	I	BSINPDS16	SBus Reset
sb_lerr_	133	I	BSINPDT	SBus Late Error (INT15)
sb_clk	142	I	BSCLOCK	SBus Clock Input
sb_rd	106	B	BSIOPD12H	SBus Read/Write
sb_sel_	135	I	BSINPDH	SBus Select
sb_d_irq_	104	O	BSIOPD12U25T	SBus Interrupt for SCSI transfers (open-drain)
sb_e_irq_	19	O	BSIOPD12U25T	SBus Interrupt for ETHERNET transfers (open-drain)
sb_p_irq_	18	0	BSIOPD12U25T	SBus Interrupt for Parallel Port Transfers (open-drain)
sb_siz[2]	138	B	BSIOPD12H	SBus Transfer Size
sb_siz[1]	139	B	BSIOPD12H	SBus Transfer Size
sb_siz[0]	140	B	BSIOPD12H	SBus Transfer Size
sb_as_	136	I	BSINPDH	SBus Address Strobe (address is valid)
chip_sel[1]	134	I	BSINPDT	High order physical address bit
sb_pa[w]	144	I	BSINPDH	High order physical address bit
sb_pa[x]	145	I	BSIONPD4H	High order physical address bit
sb_pa[y]	146	I	BSINPDH	High order physical address bit
sb_pa[5]	152	I	BSINPDH	Low order physical address bit
sb_pa[4]	147	I	BSINPDH	Low order physical address bit
sb_pa[3]	148	I	BSINPDH	Low order physical address bit
sb_pa[2]	149	I	BSINPDH	Low order physical address bit
sb_pa[1]	150	I	BSINPDH	Low order physical address bit

Table 2-4 Pinout by Function (Continued)

Name	Pin	Direction	Type	Description
sb_pa[0]	151	I	BSINPDT	Low order physical address bit
Ethernet Interface: 8 pins				
enet_aui_[2]	56	O	BSOTPD4	Ethernet TP/AUI_ select
enet_tx	57	O	BSOTPD4	Ethernet Transmit data
enet_tena	58	O	BSOTPD4	Ethernet Transmit enable
enet_clsn	59	I	BSINPDT	Ethernet Collision detect
enet_rx	60	I	BSINPDT	Ethernet Receive data
enet_rena	61	I	BSINPDT	Ethernet Receiver enable (carrier sense)
enet_tclk	62	I	BSINPDT	Ethernet Transmit clock
enet_rclk	63	I	BSINPDT	Ethernet Receive clock
SCSI Interface[3]: 20 pins				
scsi_d_[7]	79	B	SCSIPAD	SCSI Data
scsi_d_[6]	78	B	SCSIPAD	SCSI Data
scsi_d_[5]	77	B	SCSIPAD	SCSI Data
scsi_d_[4]	76	B	SCSIPAD	SCSI Data
scsi_d_[3]	74	B	SCSIPAD	SCSI Data
scsi_d_[2]	73	B	SCSIPAD	SCSI Data
scsi_d_[1]	72	B	SCSIPAD	SCSI Data
scsi_d_[0]	71	B	SCSIPAD	SCSI Data
scsi_dp_	80	B	SCSIPAD	SCSI Data Parity
scsi_sel_	82	B	SCSIPAD	SCSI Select
scsi_bsy_	83	B	SCSIPAD	SCSI Busy
scsi_req_	84	B	SCSIPADF	SCSI Request
scsi_ack_	85	B	SCSIPADF	SCSI Acknowledge
scsi_msg_	87	B	SCSIPAD	SCSI Message
scsi_c_d_	88	B	SCSIPAD	SCSI Command/Data
scsi_i_o_	89	B	SCSIPAD	SCSI Input/Output
scsi_atn_	90	B	SCSIPADF	SCSI Attention
scsi_rst_	91	B	SCSIPAD	SCSI Reset
scsi_xtal_in	96	I	OSC1401	SCSI Clock Crystal In (can drive with external CMOS clock)

Table 2-4 Pinout by Function (Continued)

Name	Pin	Direction	Type	Description
scsi_xtal_out	95	O	BSOSC1401	SCSI Clock Crystal Out (must not connect to any external load)
Parallel Port Interface: 22 Pins				
p_data[7]	25	T	BSIOPD4T	Parallel Port Data Bus
p_data[6]	26	T	BSIOPD4T	Parallel Port Data Bus
p_data[5]	28	T	BSIOPD4T	Parallel Port Data Bus
p_data[4]	29	T	BSIOPD4T	Parallel Port Data Bus
p_data[3]	31	T	BSIOPD4T	Parallel Port Data Bus
p_data[2]	32	T	BSIOPD4T	Parallel Port Data Bus
p_data[1]	34	T	BSIOPD4T	Parallel Port Data Bus
p_data[0]	35	T	BSIOPD4T	Parallel Port Data Bus
p_d_strb	23	B	BSIOPPD4D25T	Parallel Port Data Strobe (25 uA pull-down)
p_bsy_	22	B	BSIOPPD4U25T	Parallel Port Busy (25 uA pull-up)
p_ack	21	B	BSIOPPD4D25T	Parallel Port Acknowledge (25 uA pull-down)
p_pe_	39	B	BSIONPD4T	Parallel Port Paper Error
p_slct_	38	B	BSIONPD4T	Parallel Port Select
p_error	37	I	BSINPDT	Parallel Port Error
p_init	42	O	BSOTPD4	Parallel Port Initialize
p_slct_in	40	O	BSOTPD4	Parallel Port Select In
p_afxn	41	O	BSOTPD4	Parallel Port Auto Feed
p_ds_dir[4]	45	O	BSOTPD4	Parallel Port Data Strobe Direction
p_bsy_dir[4]	44	O	BSOTPD4	Parallel Port Busy Direction
p_ack_dir[4]	43	O	BSOTPD4	Parallel Port Acknowledge Direction
p_d_dir[4]	46	O	BSOTPD4	Parallel Port Data Direction

Table 2-4 Pinout by Function (Continued)

Name	Pin	Direction	Type	Description
id_cs_	14	O	BSIOPPD4U25T	Secondary Device Select (boot prom) output; pull low to specify absence of external prom
Test: 5 pins				
jtag_tdo	64	O	NCROTPD4	JTAG Test Data Output
jtag_tdi	66	I	NCRIPPDU100	JTAG Test Data Input (100 uA pull-up)
jtag_clk	65	I	NCRINPD	JTAG Clock
jtag_tms	67	I	NCRIPPDU100	JTAG Test Mode Select (100 uA pull-up)
jtag_rst_	68	I	NCRIPPDU100	JTAG Reset (100 uA pull-up)
General Purpose Oscillators[5]: 9 pins				
scc_xtal20_in	99	I	OSC1401	SCC Clock Crystal In (19.66 MHz) (can drive with external CMOS clock)
scc_xtal20_out	100	O	OSC1401	SCC Clock Crystal Out (19.66 MHz) (must not connect to any external load)
scc_clk20	101	O	OPD16SYM	SCC Clock Out (19.66 MHz)
fpy_xtal24_in	50	I	OSC1401	Floppy Clock Crystal In (24 MHz) (can drive with external CMOS clock)
fpy_xtal24_out	49	O	OSC1401	Floppy Clock Crystal Out (24 MHz) (must not connect to any external load)
fpy_clk24	48	O	OPD16SYM	Floppy Clock Out (24 MHz)
fpy_xtal32_in	52	I	OSC1401	Floppy Clock Crystal In (32 MHz) (can drive with external CMOS clock)
fpy_xtal32_out	53	O	OSC1401	Floppy Clock Crystal Out (32 MHz) (must not connect to any external load)
fpy_clk32	54	O	OPD16SYM	Floppy Clock Out (32 MHz)
Power, Ground: 37 pins				

Table 2-4 Pinout by Function (Continued)

Name	Pin	Direction	Type	Description
VDD	7	—		Power Connection
VDD	17	—		Power Connection
VDD	24	—		Power Connection
VDD	27	—		Power Connection
VDD	33	—		Power Connection
VDD	51	—		Power Connection
VDD	97	—		Power Connection
VDD	98	—		Power Connection
VDD	105	—		Power Connection
VDD	114	—		Power Connection
VDD	124	—		Power Connection
VDD	141	—		Power Connection
VDD	156	—		Power Connection
VSS	3	—		Ground Connection
VSS	13	—		Ground Connection
VSS	15	—		Ground Connection
VSS	20	—		Ground Connection
VSS	30	—		Ground Connection
VSS	36	—		Ground Connection
VSS	47	—		Ground Connection
VSS	55	—		Ground Connection
VSS	69	—		Ground Connection
VSS	70	—		Ground Connection
VSS	75	—		Ground Connection
VSS	81	—		Ground Connection
VSS	86	—		Ground Connection
VSS	92	—		Ground Connection
VSS	93	—		Ground Connection
VSS	94	—		Ground Connection
VSS	102	—		Ground Connection
VSS	103	—		Ground Connection
VSS	107	—		Ground Connection
VSS	112	—		Ground Connection
VSS	117	—		Ground Connection

Table 2-4 Pinout by Function (Continued)

Name	Pin	Direction	Type	Description
VSS	127	—		Ground Connection
VSS	143	—		Ground Connection
VSS	158	—		Ground Connection

1. The chip_sel pin is an additional qualifier (active high) to the sb_sel_ line. In some system configurations where the 89C100 and the 89C105 share a single SBus select line, PA[27] can be used to select between the two.
2. Drives MIS input of the AT&T T7213 chip to select between twisted pair and AUI-type Ethernet interfaces, with ENET_AUI_ = 0 selecting AUI.
3. All of the SCSI pads (except the crystal oscillator pads) are custom NCR 48 mA bidirectional open-drain pads with hysteresis on inputs.
4. The Parallel Port control and data line direction bits, (for example, p_*_dir), are gang programmed by the DIR bit of the Transfer Control Register. DIR=0 sets transfer direction away from the 89C100 (p_d_dir=p_ds_dir=1; p_bsy_dir=p_ack_dir=0); DIR=1 sets transfer direction towards the 89C100 (p_d_dir=p_ds_dir=0; p_bsy_dir=p_ack_dir=1).
5. In some system configurations, the 89C100 provides these three clocks to the 89C105 (which is pin limited). These are really general-purpose 20-50 MHz crystal oscillator pads that can operate in both fundamental and overtone mode. Refer to page 60“OSC1401 Crystal Oscillator” for more information.

Pinout by Pin Number Sequence

Table 2-5 Pinout by Pin Number Sequence

Pin	Name	Direction	Type	Description
1	sb_d[22]	B	BSIOPD12S16	SBus Data Bus
2	sb_d[23]	B	BSIOPD12S16	SBus Data Bus
3	VSS	—		Ground Connection
4	sb_d[24]	B	BSIOPD12S16	SBus Data Bus
5	sb_d[25]	B	BSIOPD12S16	SBus Data Bus
6	sb_d[26]	B	BSIOPD12S16	SBus Data Bus
7	VDD	—		Power Connection
8	sb_d[27]	B	BSIOPD12S16	SBus Data Bus
9	sb_d[28]	B	BSIOPD12S16	SBus Data Bus
10	sb_d[29]	B	BSIOPD12S16	SBus Data Bus
11	sb_d[30]	B	BSIOPD12S16	SBus Data Bus
12	sb_d[31]	B	BSIOPD12S16	SBus Data Bus (MSB)
13	VSS	—		Ground Connection
14	id_cs_	O	BSIOPPD4U25T	Secondary Device Select (boot prom) output; pull low to specify absence of external prom
15	VSS	—		Ground Connection
16	sb_reset_	I	BSINPDS16	SBus Reset
17	VDD	—		Power Connection
18	sb_p_irq_	O	BSIOPD12U25T	SBus Interrupt for Parallel Port Transfers (open-drain)
19	sb_e_irq_	O	BSIOPD12U25T	SBus Interrupt for Ethernet transfers (open-drain)
20	VSS	—		Ground Connection
21	p_ack	B	BSIOPPD4D25T	Parallel Port Acknowledge (25 µA pull-down)
22	p_bsy_	B	BSIOPPD4U25T	Parallel Port Busy (25 µA pull-up)
23	p_d_strb	B	BSIOPPD4D25T	Parallel Port Data Strobe (25 µA pull-down)
24	VDD	—		Power Connection
25	p_data[7]	T	BSIOPD4T	Parallel Port Data Bus
26	p_data[6]	T	BSIOPD4T	Parallel Port Data Bus
27	VDD	—		Power Connection

Table 2-5 Pinout by Pin Number Sequence (Continued)

Pin	Name	Direction	Type	Description
28	p_data[5]	T	BSIOPD4T	Parallel Port Data Bus
29	p_data[4]	T	BSIOPD4T	Parallel Port Data Bus
30	VSS	—		Ground Connection
31	p_data[3]	T	BSIOPD4T	Parallel Port Data Bus
32	p_data[2]	T	BSIOPD4T	Parallel Port Data Bus
33	VDD	—		Power Connection
34	p_data[1]	T	BSIOPD4T	Parallel Port Data Bus
35	p_data[0]	T	BSIOPD4T	Parallel Port Data Bus
36	VSS	—		Ground Connection
37	p_error	I	BSINPDT	Parallel Port Error
38	p_slct_	B	BSIONPD4T	Parallel Port Select
39	p_pe_	B	BSIONPD4T	Parallel Port Paper Error
40	p_slct_in	O	BSOTPD4	Parallel Port Select In
41	p_afxn	O	BSOTPD4	Parallel Port Auto Feed
42	p_init	O	BSOTPD4	Parallel Port Initialize
43	p_ack_dir[1]	O	BSOTPD4	Parallel Port Acknowledge Direction
44	p_bsy_dir[1]	O	BSOTPD4	Parallel Port Busy Direction
45	p_ds_dir[1]	O	BSOTPD4	Parallel Port Data Strobe Direction
46	p_d_dir[1]	O	BSOTPD4	Parallel Port Data Direction
47	VSS	—		Ground Connection
48	fpy_clk24[2]	O	OPD16SYM	Floppy Clock Out (24 MHz)
49	fpy_xtal24_out[2]	O	OSC1401	Floppy Clock Crystal Out (24 MHz) (must not connect to any external load)
50	fpy_xtal24_in[2]	I	OSC1401	Floppy Clock Crystal In (24 MHz) (can drive with external CMOS clock)
51	VDD	—		Power Connection
52	fpy_xtal32_in[2]	I	OSC1401	Floppy Clock Crystal In (32 MHz) (can drive with external CMOS clock)
53	fpy_xtal32_out[2]	O	OSC1401	Floppy Clock Crystal Out (32 MHz) (must not connect to any external load)
54	fpy_clk32[2]	O	OPD16SYM	Floppy Clock Out (32 MHz)

Table 2-5 Pinout by Pin Number Sequence (Continued)

Pin	Name	Direction	Type	Description
55	VSS	—		Ground Connection
56	enet_aui_[3]	O	BSOTPD4	Ethernet TP/AUI_ select output
57	enet_tx	O	BSOTPD4	Ethernet Transmit data output
58	enet_tena	O	BSOTPD4	Ethernet Transmit enable output
59	enet_clsn	I	BSINPDT	Ethernet Collision detect input
60	enet_rx	I	BSINPDT	Ethernet Receive data input
61	enet_rena	I	BSINPDT	Ethernet Receiver enable (carrier sense) input
62	enet_tclk	I	BSINPDT	Ethernet Transmit clock input
63	enet_rclk	I	BSINPDT	Ethernet Receive clock input
64	jtag_tdo	O	NCROTPD4	JTAG Test Data Output
65	jtag_clk	I	NCRINPD	JTAG Clock
66	jtag_tdi	I	NCRIPPDU100	JTAG Test Data Input (100 μA pull-up)
67	jtag_tms	I	NCRIPPDU100	JTAG Test Mode Select (100 μA pull-up)
68	jtag_rst_	I	NCRIPPDU100	JTAG Reset (100 μA pull-up)
69	VSS	—		Ground Connection
70	VSS	—		Ground Connection
71	scsi_d_[0][4]	B	SCSIPAD	SCSI Data
72	scsi_d_[1][4]	B	SCSIPAD	SCSI Data
73	scsi_d_[2][4]	B	SCSIPAD	SCSI Data
74	scsi_d_[3][4]	B	SCSIPAD	SCSI Data
75	VSS	—		Ground Connection
76	scsi_d_[4][4]	B	SCSIPAD	SCSI Data
77	scsi_d_[5][4]	B	SCSIPAD	SCSI Data
78	scsi_d_[6][4]	B	SCSIPAD	SCSI Data
79	scsi_d_[7][4]	B	SCSIPAD	SCSI Data
80	scsi_dp_[4]	B	SCSIPAD	SCSI Data Parity
81	VSS	—		Ground Connection
82	scsi_sel_[4]	B	SCSIPAD	SCSI Select
83	scsi_bsy_[4]	B	SCSIPAD	SCSI Busy

Table 2-5 Pinout by Pin Number Sequence (Continued)

Pin	Name	Direction	Type	Description
84	scsi_req_[4]	B	SCSIPADF	SCSI Request
85	scsi_ack_[4]	B	SCSIPADF	SCSI Acknowledge
86	VSS	—		Ground Connection
87	scsi_msg_[4]	B	SCSIPAD	SCSI Message
88	scsi_c_d_[4]	B	SCSIPAD	SCSI Command/Data
89	scsi_i_o_[4]	B	SCSIPAD	SCSI Input/Output
90	scsi_atn_[4]	B	SCSIPADF	SCSI Attention
91	scsi_rst_[4]	B	SCSIPAD	SCSI Reset
92	VSS	—		Ground Connection
93	VSS	—		Ground Connection
94	VSS	—		Ground Connection
95	scsi_xtal_out	O	OSC1401	SCSI Clock Crystal Out (must not connect to any external load)
96	scsi_xtal_in	I	BSOSC1401	SCSI Clock Crystal In (can drive with external CMOS clock)
97	VDD	—		Power Connection
98	VDD	—		Power Connection
99	scc_xtal20_in[2]	I	OSC1401	SCC Clock Crystal In (19.66 MHz) (can drive with external CMOS clock)
100	scc_xtal20_out[2]	O	OSC1401	SCC Clock Crystal Out (19.66 MHz) (must not connect to any external load)
101	scc_clk20[2]	O	OPD16SYM	SCC Clock Out (19.66 MHz)
102	VSS	—		Ground Connection
103	VSS	—		Ground Connection
104	sb_d_irq_	O	BSIOPD12U25T	SBus Interrupt for SCSI transfers (open-drain)
105	VDD	—		Power Connection
106	sb_rd	T	BSIOPD12H	SBus Read/Write
107	VSS	—		Ground Connection
108	sb_d[0]	B	BSIOPD12S16	SBus Data Bus (LSB)
109	sb_d[1]	B	BSIOPD12S16	SBus Data Bus
110	sb_d[2]	B	BSIOPD12S16	SBus Data Bus
111	sb_d[3]	B	BSIOPD12S16	SBus Data Bus

Table 2-5 Pinout by Pin Number Sequence (Continued)

Pin	Name	Direction	Type	Description
112	VSS	—		Ground Connection
113	sb_d[4]	B	BSIOPD12S16	SBus Data Bus
114	VDD	—		Power Connection
115	sb_d[5]	B	BSIOPD12S16	SBus Data Bus
116	sb_d[6]	B	BSIOPD12S16	SBus Data Bus
117	VSS	—		Ground Connection
118	sb_d[7]	B	BSIOPD12S16	SBus Data Bus
119	sb_d[8]	B	BSIOPD12S16	SBus Data Bus
120	sb_d[9]	B	BSIOPD12S16	SBus Data Bus
121	sb_d[10]	B	BSIOPD12S16	SBus Data Bus
122	sb_d[11]	B	BSIOPD12S16	SBus Data Bus
123	sb_d[12]	B	BSIOPD12S16	SBus Data Bus
124	VDD	—		Power Connection
125	sb_d[13]	B	BSIOPD12S16	SBus Data Bus
126	sb_d[14]	B	BSIOPD12S16	SBus Data Bus
127	VSS	—		Ground Connection
128	sb_d[15]	B	BSIOPD12S16	SBus Data Bus
129	sb_ack[2]	B	BSIOPD12H	SBus Acknowledge
130	sb_ack[1]	B	BSIOPD12I	SBus Acknowledge
131	sb_br_	B	BSIOPD12T	SBus Bus Request
132	sb_bg_	I	BSINPDH	SBus Bus Grant
133	sb_lerr_	I	BSINPDT	SBus Late Error (INT15)
134	chip_sel[5]	I	BSINPDT	High order physical address bits (for slave decodes)
135	sb_sel_	I	BSINPDH	SBus Select
136	sb_as_	I	BSINPDH	SBus Address Strobe (address is valid)
137	sb_ack[0]	B	BSIOPD12I	SBus Acknowledge
138	sb_siz[2]	B	BSIOPD12H	SBus Transfer Size
139	sb_siz[1]	B	BSIOPD12H	SBus Transfer Size
140	sb_siz[0]	B	BSIOPD12H	SBus Transfer Size
141	VDD	—		Power Connection
142	sb_clk	I	BSINPDH	SBus Clock Input
143	VSS	—		Ground Connection

Table 2-5 Pinout by Pin Number Sequence (Continued)

Pin	Name	Direction	Type	Description
144	sb_pa_w	I	BSINPDH	High order physical address bit
145	sb_pa_x	I	BSIONPD4H	High order physical address bit
146	sb_pa_y	I	BSINPDH	High order physical address bit
147	sb_pa[4]	I	BSINPDH	Low order physical address bit
148	sb_pa[3]	I	BSINPDH	Low order physical address bit
149	sb_pa[2]	I	BSINPDH	Low order physical address bit
150	sb_pa[1]	I	BSINPDH	Low order physical address bit
151	sb_pa[0]	I	BSINPDT	Low order physical address bit
152	sb_pa[5]	I	BSINPDT	Low order physical address bit
153	sb_d[16]	B	BSIOPD12S16	SBus Data Bus
154	sb_d[17]	B	BSIOPD12S16	SBus Data Bus
155	sb_d[18]	B	BSIOPD12S16	SBus Data Bus
156	VDD	—		Power Connection
157	sb_d[19]	B	BSIOPD12S16	SBus Data Bus
158	VSS	—		Ground Connection
159	sb_d[20]	B	BSIOPD12S16	SBus Data Bus
160	sb_d[21]	B	BSIOPD12S16	SBus Data Bus

1. The Parallel Port control and data line direction bits, (for example, - p_*_dir), are gang programmed by the DIR bit of the Transfer Control Register. DIR=0 sets transfer direction away from the 89C100 (p_d_dir=p_ds_dir=1; p_bsy_dir=p_ack_dir=0); DIR=1 sets transfer direction towards the 89C100 (p_d_dir=p_ds_dir=0; p_bsy_dir=p_ack_dir=1).
2. In some system configurations, the 89C100 provides these three clocks to the 89C105 (which is pin limited). These are really general-purpose 20-50 MHz crystal oscillator pads that can operate in both fundamental and overtone mode. Refer to page 60, “OSC1401 Crystal Oscillator” for more information.
3. Drives MIS input of the AT&T T7213 chip to select between twisted pair and AUI-type Ethernet interfaces, with ENET_AUI_ = 0 selecting AUI.
4. All of the SCSI pads are custom NCR 48 mA bidirectional open-drain pads with hysteresis on inputs.
5. The chip_sel pin is an additional qualifier (active high) to the sb_sel_ line. In some system configurations, where the 89C100 and the 89C105 share a single SBus select line, PA[27] is used to select between the two, with PA[27]=1 selecting the 89C100.

JTAG Boundary Information

Table 2-6 describes the boundary scan chain. The numbers listed in the Input, Output, and Enable columns represent the bit order of the scan chain. Bit 0 is the first to be scanned in. All of the enable signals are active low.

Table 2-6 Boundary Chain Description

Pin	Name	Type	Input	Output	Enable
1	sb_d[22]	BIDIR	87	88	97
2	sb_d[23]	BIDIR	89	90	97
3	io_vss	POWER	—	—	—
4	sb_d[24]	BIDIR	91	92	97
5	sb_d[25]	BIDIR	93	94	97
6	sb_d[26]	BIDIR	95	96	97
7	io_vdd	POWER	—	—	—
8	sb_d[27]	BIDIR	98	99	97
9	sb_d[28]	BIDIR	100	101	97
10	sb_d[29]	BIDIR	102	103	97
11	sb_d[30]	BIDIR	104	105	97
12	sb_d[31]	BIDIR	106	107	97
13	io_vss	POWER	—	—	—
14	id_cs_	BIDIR	109	110	108
15	core_vss	POWER	—	—	—
16	sb_reset_	INPUT	111	—	—
17	core_vdd	POWER	—	—	—
18	sb_p_irq_	BIDIR	113	114	112
19	sb_e_irq_	BIDIR	116	117	115
20	core_vss	POWER	—	—	—
21	p_ack	BIDIR	120	121	118
22	p_bsy_	BIDIR	123	124	122
23	p_d_strb	BIDIR	126	127	125
24	core_vdd	POWER	—	—	—
25	p_data[7]	BIDIR	128	129	136
26	p_data[6]	BIDIR	130	131	136
27	io_vdd	POWER	—	—	—
28	p_data[5]	BIDIR	132	133	136
29	p_data[4]	BIDIR	134	135	136
30	core_vss	POWER	—	—	—

Table 2-6 Boundary Chain Description (Continued)

Pin	Name	Type	Input	Output	Enable
31	p_data[3]	BIDIR	137	138	136
32	p_data[2]	BIDIR	139	140	136
33	core_vdd	POWER	—	—	—
34	p_data[1]	BIDIR	142	143	136
35	p_data[0]	BIDIR	144	145	136
36	io_vss	POWER	—	—	—
37	p_error	INPUT	146	—	—
38	p_slct_	BIDIR	147	148	119
39	p_pe_	BIDIR	149	150	119
40	p_slct_in	TRISTATE	—	152	151
41	p_afxn	TRISTATE	—	153	155
42	p_init	TRISTATE	—	154	155
43	p_ack_dir	TRISTATE	—	156	155
44	p_bsy_dir	TRISTATE	—	158	157
45	p_ds_dir	TRISTATE	—	159	141
46	p_d_dir	TRISTATE	—	160	155
47	io_vss	POWER	—	—	—
48	fpy_clk24	OUTPUT	—	—	—
49	fpy_xtal24_out	OUTPUT	—	—	—
50	fpy_xtal24_in	INPUT	—	—	—
51	io_vdd	POWER	—	—	—
52	fpy_xtal32_in	INPUT	—	—	—
53	fpy_xtal32_out	OUTPUT	—	—	—
54	fpy_clk32	OUTPUT	—	—	—
55	io_vss	POWER	—	—	—
56	enet_aui_	TRISTATE	—	162	161
57	enet_tx	TRISTATE	—	163	141
58	enet_tena	TRISTATE	—	164	141
59	enet_clsn	INPUT	165	—	—
60	enet_rx	INPUT	166	—	—
61	enet_rena	INPUT	167	—	—
62	enet_tclk	INPUT	168	—	—
63	enet_rclk	INPUT	169	—	—
64	jtag_tdo	TDO	—	—	—

Table 2-6 Boundary Chain Description (Continued)

Pin	Name	Type	Input	Output	Enable
65	jtag_clk	TCK	—	—	—
66	jtag_tdi	TDI	—	—	—
67	jtag_tms	TMS	—	—	—
68	jtag_rst_	TRSTB	—	—	—
69	io_vss	POWER	—	—	—
70	scsipad_gnd	POWER	—	—	—
71	scsi_d[0]	BIDIR	170	171	188
72	scsi_d[1]	BIDIR	172	173	188
73	scsi_d[2]	BIDIR	174	175	188
74	scsi_d[3]	BIDIR	176	177	188
75	scsipad_gnd	POWER	—	—	—
76	scsi_d[4]	BIDIR	178	179	188
77	scsi_d[5]	BIDIR	180	181	188
78	scsi_d[6]	BIDIR	182	183	188
79	scsi_d[7]	BIDIR	184	185	188
80	scsi_dp_	BIDIR	186	187	188
81	scsipad_gnd	POWER	—	—	—
82	scsi_sel_	BIDIR	194	195	208
83	scsi_bsy_	BIDIR	196	197	208
84	scsi_req_	BIDIR	189	190	193
85	scsi_ack_	BIDIR	191	192	193
86	scsipad_gnd	POWER	—	—	—
87	scsi_msg_	BIDIR	198	199	208
88	scsi_c_d_	BIDIR	200	201	208
89	scsi_i_o_	BIDIR	202	203	208
90	scsi_atn_	BIDIR	204	205	208
91	scsi_rst_	BIDIR	206	207	208
92	scsipad_gnd	POWER	—	—	—
93	core_vss	POWER	—	—	—
94	io_vss	POWER	—	—	—
95	scsi_xtal_out	OUTPUT	—	—	—
96	scsi_xtal_in	INPUT	0	—	—
97	io_vdd	POWER	—	—	—
98	core_vdd	POWER	—	—	—

Table 2-6 Boundary Chain Description (Continued)

Pin	Name	Type	Input	Output	Enable
99	scc_xtal20_in	INPUT	—	—	—
100	scc_xtal20_out	OUTPUT	—	—	—
101	scc_clk20	OUTPUT	—	—	—
102	io_vss	POWER	—	—	—
103	core_vss	POWER	—	—	—
104	sb_d_irq_	BIDIR	2	3	1
105	core_vdd	POWER	—	—	—
106	sb_rd	BIDIR	5	6	4
107	io_vss	POWER	—	—	—
108	sb_d[0]	BIDIR	7	8	15
109	sb_d_[1]	BIDIR	9	10	15
110	sb_d[2]	BIDIR	11	12	15
111	sb_d[3]	BIDIR	13	14	15
112	core_vss	POWER	—	—	—
113	sb_d[4]	BIDIR	16	17	15
114	io_vdd	POWER	—	—	—
115	sb_d[5]	BIDIR	18	19	15
116	sb_d[6]	BIDIR	20	21	15
117	io_vss	POWER	—	—	—
118	sb_d[7]	BIDIR	22	23	30
119	sb_d[8]	BIDIR	24	25	30
120	sb_d[9]	BIDIR	26	27	30
121	sb_d[10]	BIDIR	28	29	30
122	sb_d[11]	BIDIR	31	32	30
123	sb_d[12]	BIDIR	33	34	30
124	io_vdd	POWER	—	—	—
125	sb_d[13]	BIDIR	35	36	30
126	sb_d[14]	BIDIR	37	38	70
127	io_vss	POWER	—	—	—
128	sb_d[15]	BIDIR	39	40	70
129	sb_ack[2]	BIDIR	41	42	43
130	sb_ack[1]	BIDIR	44	45	43
131	sb_br_	BIDIR	46	47	141
132	sb_bg_	INPUT	48	—	—

Table 2-6 Boundary Chain Description (Continued)

Pin	Name	Type	Input	Output	Enable
133	sb_lerr_	INPUT	49	—	—
134	chip_sel	INPUT	50	—	—
135	sb_sel_	INPUT	51	—	—
136	sb_as_	INPUT	52	—	—
137	sb_ack[0]	BIDIR	54	55	53
138	sb_size[2]	BIDIR	56	57	58
139	sb_size[1]	BIDIR	59	60	58
140	sb_size[0]	BIDIR	61	62	58
141	io_vdd	POWER	—	—	—
142	sb_clk	INPUT	63	—	—
143	io_vss	POWER	—	—	—
144	sb_pa_w	INPUT	64	—	—
145	sb_pa_x	BIDIR	65	66	119
146	sb_p_y	INPUT	67	—	—
147	sb_pa[4]	INPUT	68	—	—
148	sb_pa[3]	INPUT	69	—	—
149	sb_pa[2]	INPUT	71	—	—
150	sb_pa[1]	INPUT	72	—	—
151	sb_pa[0]	INPUT	73	—	—
152	sb_pa[5]	INPUT	74	—	—
153	sb_d[16]	BIDIR	75	76	70
154	sb_d[17]	BIDIR	77	78	70
155	sb_d[18]	BIDIR	79	80	70
156	io_vdd	POWER	—	—	—
157	sb_d[19]	BIDIR	81	82	70
158	io_vss	POWER	—	—	—
159	sb_d[20]	BIDIR	83	84	70
160	sb_d[21]	BIDIR	85	86	70

Functional Operation

This section includes the following:

- Detailed chip block diagram
- Chip-level address map
- Functional chip description

Detailed Chip Block Diagram

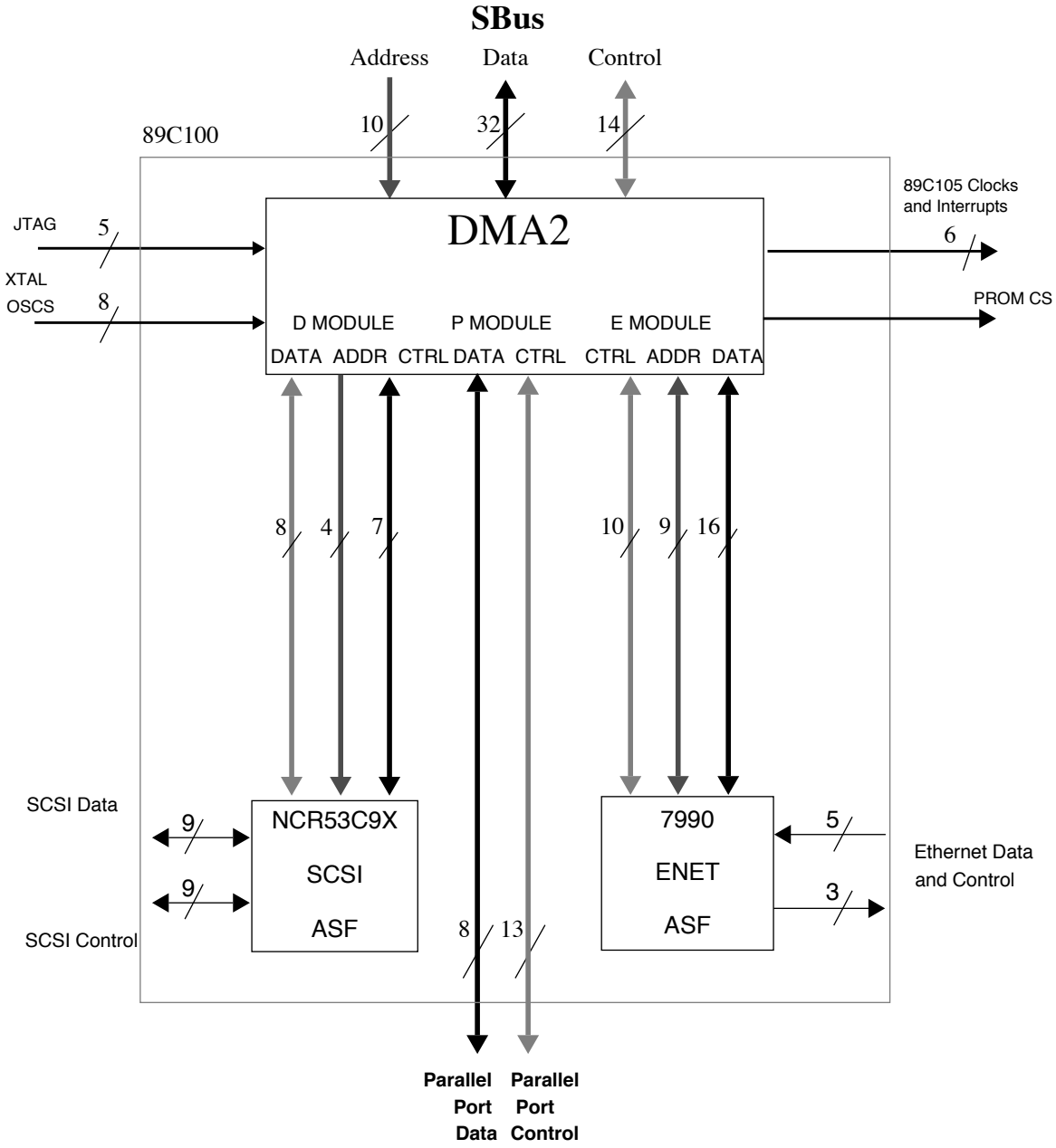


Figure 2-3 Chip Block Diagram

Chip-Level Address Map

Table 2-7 Chip-Level Address Map

sb_pa(27:0)[1] [2]	Register Accesses	Type	Size
0x800 0000	**DMA2 Internal ID Register[3]**	R	32
0x840 0000 -> 0x840 000f	**DMA2 ESP Registers**		
0x840 0000	Control/Status Register (D_CSR)	R/W	32
0x840 0004	Address Register (D_ADDR)[4]	R/W	32
0x840 0008	Byte Count Register (D_BCNT)[4]	R/W	24
0x840 000c	Test Control/Status Reg (D_TST_CSR)	R/W	32
0x840 0010 -> 0x840 001f	**DMA2 Ethernet Registers**		
0x840 0010	Control/Status Register (E_CSR)	R/W	32
0x840 0014	Test Control/Status Register (E_TST_CSR)	R/W	32
0x840 0018	Cache Valid Bits (E_VLD)	R/W	32
0x840 001c	Base Address Reg (E_BASE_ADDR)	R/W	8
0xc80 0000 -> 0xc80 001f	**DMA2 Parallel Port Registers**		
0xc80 0000	Control/Status Register (P_CSR)	R/W	32
0xc80 0004	Address Register (P_ADDR)[5]	R/W	32
0xc80 0008	Byte Count Register (P_BCNT)[5]	R/W	32
0xc80 000c	Test Control/Status Register (P_TST_CSR)	R/W	32
0xc80 0010	Hardware Configuration Reg (P_HCR)	R/W	16
0xc80 0012	Operation Configuration Reg (P_OCR)	R/W	16
0xc80 0014	Parallel Data Register (P_DR)	R/W	8
0xc80 0015	Transfer Control Register (P_TCR)	R/W	8
0xc80 0016	Output Register (P_OR)	R/W	8
0xc80 0017	Input Register (P_IR)	R/W	8
0xc80 0018	Interrupt Control Register (P_ICR)	R/W	16

Table 2-7 Chip-Level Address Map (Continued)

sb_pa(27:0)[1] [2]	Register Accesses	Type	Size
0x880 0000 - > 0x880 003f	**SCSI Controller Registers**		
0x880 0000	Transfer Count Low (7:0)	R/W	8
0x880 0004	Transfer Count Middle (15:8)	R/W	8
0x880 0008	FIFO Data	R/W	8
0x880 000c	Command	R/W	8
0x880 0010	Status	R	8
0x880 0010	Select-Reselect Bus ID	W	8
0x880 0014	Interrupt	R	8
0x880 0014	Select-Reselect Time-Out	W	8
0x880 0018	Sequence Step	R	8
0x880 0018	Synchronous Transfer Period	W	8
0x880 001c	FIFO Flags	R	8
0x880 001c	Synchronous Offset	W	8
0x880 0020	Configuration #1	R/W	8
0x880 0024	Clock Conversion Factor	W	8
0x880 0028	Test (Chip Test Use Only)	W	8
0x880 002c	Configuration #2	R/W	8
0x880 0030	Configuration #3	R/W	8
0x880 0038	Transfer Count High (23:16)	R/W	8
0x8c0 0000 -> 0x8c0 0003	**Ethernet Controller Registers**		
0x8c0 0000	Register Data Port (RDP)	R/W	16
0x8c0 0002	Register Address Port (RAP)	R/W	16

1. (chip_sel, sb_pa_w,sb_pa_x,sb_pa_y) = sb_pa(27,26,23,22) would be the mapping for a typical system. This is the mapping shown.
2. It is recommended that software access the DMA2 registers with sb_pa[5] = 0 for future expansion.
3. Byte and 1/2 word accesses to this register are also allowed.
4. The "NEXT" Address/Byte Count registers are accessed at these addresses using the D_EN_NEXT bit in the D_CSR. Refer to “DMA2 DMA Core” for details.
5. The “NEXT” Address/Byte Count registers are accessed at these addresses using the P_EN_NEXT bit in the P_CSR. Refer to “DMA2 DMA Core” for details.

Functional Description

Overview

The 89C100 integrates the SBus DMA2 Controller, the NCR92C990 802.3 LAN Controller, and the NCR53C9X Fast SCSI Processor in a 160-pin plastic quad flat package (PQFP). The programmer's interface is identical to that of a discrete implementation using the above ICs. The chip-level address map is defined in the next section. Refer to "DMA2 DMA Core," "NCR92C990 Ethernet Core," and "NCR53C9X SCSI Core" for more information on the above devices.

89C100 and 89C105 Interdependencies

When the 89C100 and the 89C105 are used together, the 89C105 receives three clocks from the 89C100 (fpy_clk24, fpy_clk32, and scc_clk_20). The 89C100 simply provides oscillator pads on its pins because of a pin limitation on the 89C105. The 89C100 does not use these clock signals internally. The 89C100 also sends its three interrupt signals to the 89C105 for processing, they are; sb_d_irq_, sb_e_irq_, and sb_p_irq_ for; SCSI, Ethernet, and parallel port interrupts, respectively. Refer to"NCR89C105 Slave I/O" for a description of how the 89C105 handles interrupts. It is necessary to provide both enet_tclk and scsi_clk even if the Ethernet controller and SCSI controller are not used.

Technology

The 89C100 is a standard cell design, based on the NCR VS700H technology (.95µ drawn,.7 effective). It consists of 60,000 equivalent gates.

Start-Up Information

The 89C100 receives a reset from the SBus signal sb_reset_. This signal must be asserted for at least 512 SBus clock cycles after the systempower is stable, as specified by SBus specification B.0. After this, the 89C100 is ready for programming.

Functional Blocks

Overview

This section includes block diagrams, descriptions, and block-level address maps for the following:

- DMA2 Block
- SCSI Block
- Ethernet Block
- Test Block

DMA2 Block

The DMA2 block is a functionally and logically equivalent implementation of the L64854 SBus DMA controller with two minor differences.

Differences

- E_CSR bit 20, E_ALE/AS_ is not implemented. This allows use of other ENET controllers which is only an option in a discrete implementation.
- The pullup for the id_cs_ pin is provided internally. To use an external PROM simply connect id_cs_ with the PROM chip select pin. To signify absence of an external PROM connect id_cs_ to logic low.

DMA2 Block Diagram

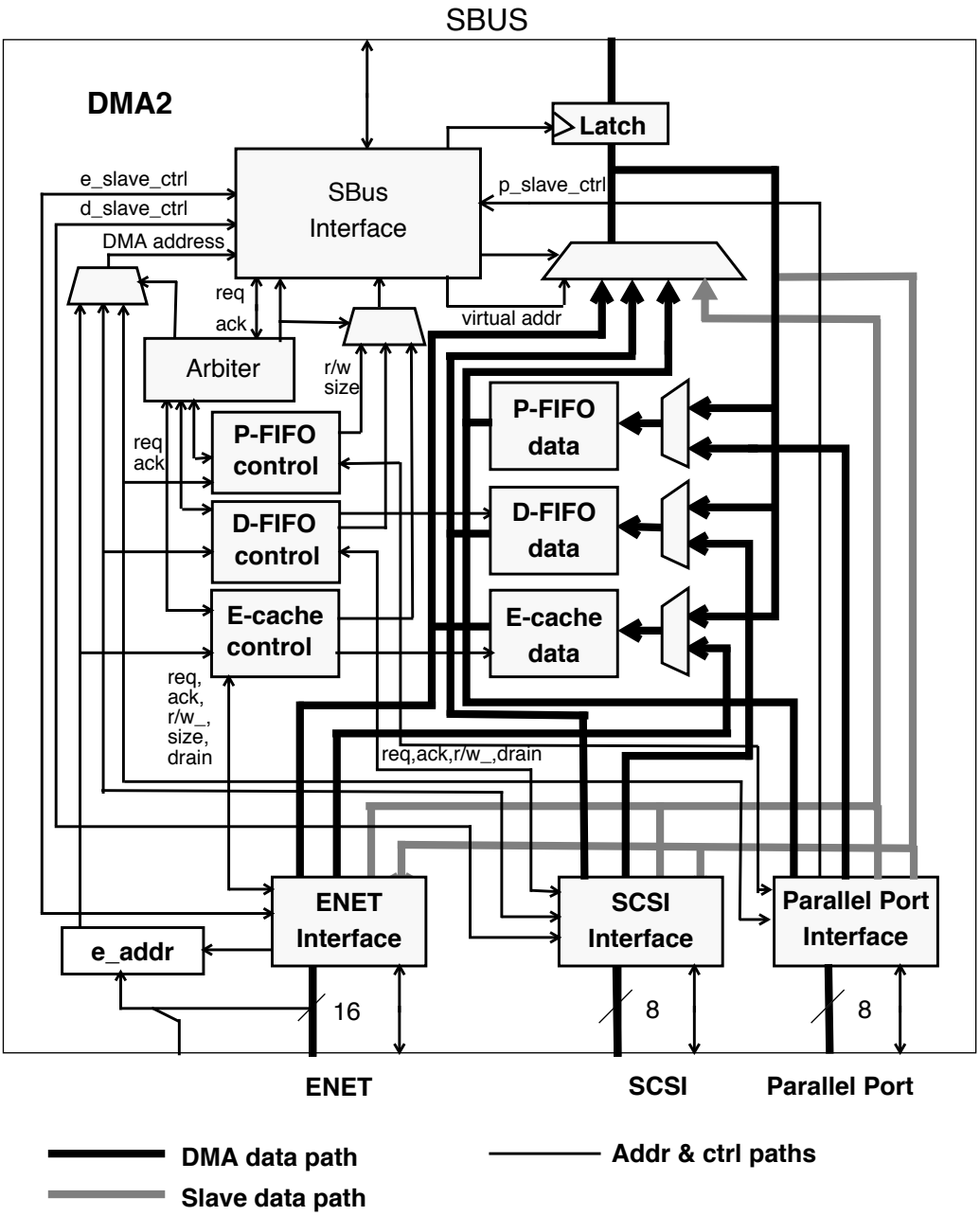


Figure 2-4 DMA2 Block Diagram

DMA2 Level Address Map

Table 2-8 DMA2 Level Address Map

sb_pa_(w,x,y)[1]	sb_pa(27:0)[2]	Register Accessed	Type	Size
000	**0x800 0000**	**Internal ID Register[3]**	R	32
	0x840 0000 -> 0x840 000f	**DMA2 ESP Registers**		
001	0x840 0000	Control/Status Register (D_CSR)	R/W	32
001	0x840 0004	Address Register (D_ADDR)[4]	R/W	32
001	0x840 0008	Byte Count Register (D_BCNT)[4]	R/W	24
001	0x840 000c	Test Control/Status Reg (D_TST_CSR)	R/W	32
	0x840 0010 -> 0x840 001f	**DMA2 Ethernet Registers**		
001	0x840 0010	Control/Status Register (E_CSR)	R/W	32
001	0x840 0014	Test Control/Status Reg (E_TST_CSR)	R/W	32
001	0x840 0018	Cache Valid Bits (E_VLD)	R/W	32
001	0x840 001c	Base Address Reg (E_BASE_ADDR)	R/W	8
	0xc80 0000 -> 0xc80 001f	**DMA2 Parallel Port Registers**		
110	0xc80 0000	Control/Status Register (P_CSR)	R/W	32
110	0xc80 0004	Address Register (P_ADDR)[5]	R/W	32
110	0xc80 0008	Byte Count Register (P_BCNT)[5]	R/W	32
110	0xc80 000c	Test Control/Status Reg (P_TST_CSR)	R/W	32
110	0xc80 0010	Hardware Configuration Reg (P_HCR)	R/W	16
110	0xc80 0012	Operation Configuration Reg (P_OCR)	R/W	16
110	0xc80 0014	Parallel Data Register (P_DR)	R/W	8
110	0xc80 0015	Transfer Control Register (P_TCR)	R/W	8
110	0xc80 0016	Output Register (P_OR)	R/W	8
110	0xc80 0017	Input Register (P_IR)	R/W	8
110	0xc80 0018	Interrupt Control Register (P_ICR)	R/W	16

1. (chip_sel,sb_pa_(w,x,y)) = sb_pa(27,26,23,22) in a typical system.
2. This column specifies a 27-bit address for systems using the same chip_sel and sb_pa_(w,x,y) mapping as described in 1.
3. Byte and 1/2 word accesses to this register are also allowed. If the id_cs_ pin is tied to ground, then addresses 0x800,0000-0x83F,FFFF all map to the internal chip ID register. If the id_cs_ pin it tied high or allowed to float (it has an internal pullup), then this address range maps to the external ID PROM.
4. The "NEXT" Address/Byte Count registers are accessed at these addresses using the D_EN_NEXT bit in the D_CSR. Refer to "DMA2 DMA Core" for details.
5. The "NEXT" Address/Byte Count registers are accessed at these addresses using the P_EN_NEXT bit in the P_CSR. Refer to "DMA2 DMA Core" for details.

SCSI Block

The SCSI block is based on the NCR53C9X ASF which is a superset of (and fully backward compatible with) the NCR53C90A previously found on SPARCstations.

Differences

The 89C100 implementation of the SCSI channel differs from former discrete implementations as follows:

- The following pins exist in the discrete implementation but not in the 89C100 chip:
  - TGS, IGS, DIFFM—Not needed for single-ended SCSI
  - RESETO—Not normally used in a system
  - All current SPARCstation designs operate as single-ended SCSI only, with the RESETO pin floating so this was chosen for the 89C100.
- The NCR53C9X ASF has two additional registers:
  - Configuration Register 3 (used to enable Fast SCSI)
  - Transfer Count High (allows for up to 16 Mbyte block transfers)
- The NCR53C9X ASF can be clocked at 40 Mhz (necessary for Fast SCSI). Software using hardware clocked at this speed will need to adjust the Clock Conversion Factor Register accordingly.

Refer to "NCR53C9X SCSI Core" for details.

SCSI Block Diagram

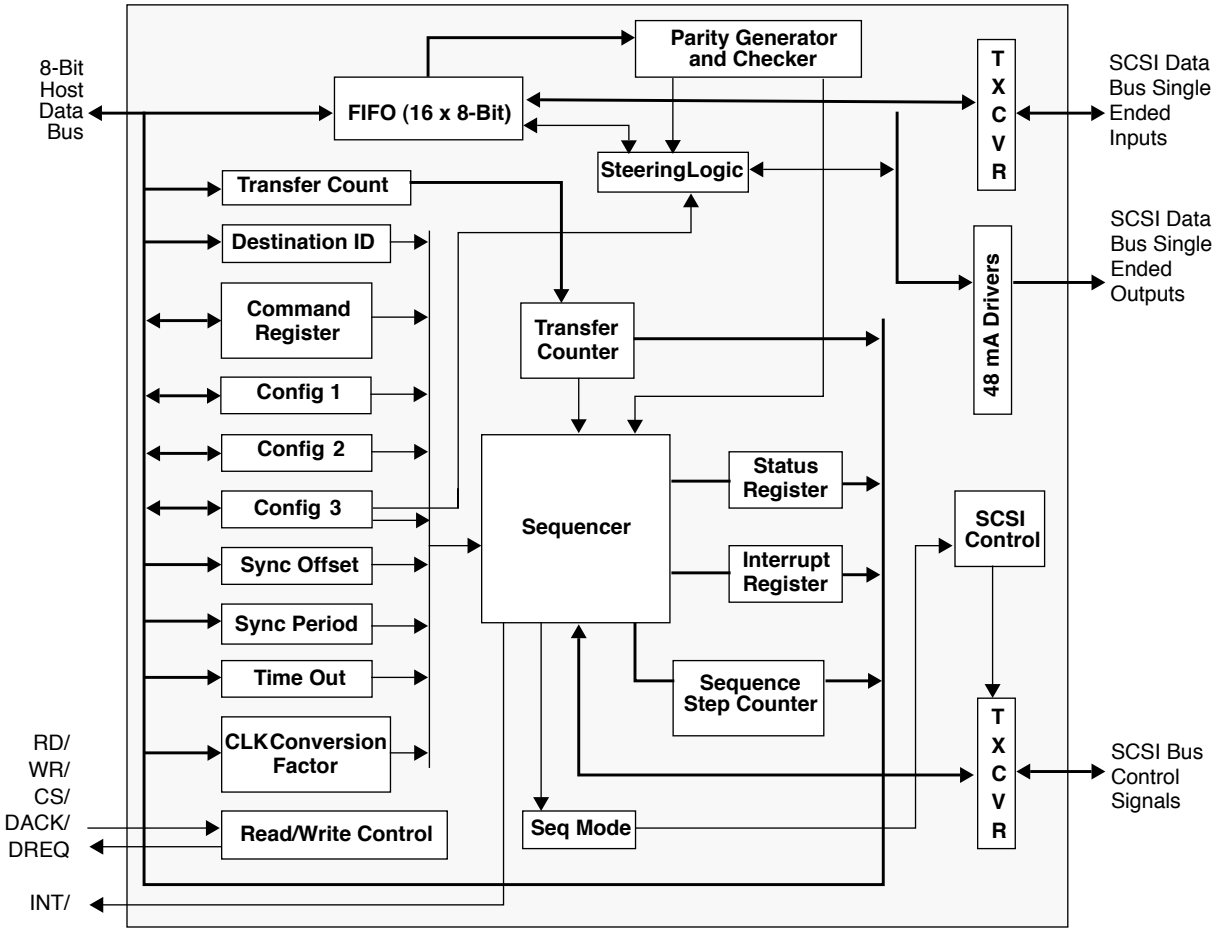


Figure 2-5 SCSI Block Diagram

SCSI-Level Address Map

Table 2-9 NCR53C9X Registers

sb_pa_(w,x,y)[1]	sb_pa(27:0)	Register Accessed	Type	Size
	0x880 0000 - > 0x880 003f	**SCSI Controller Registers**		
010	0x880 0000	Transfer Count Low (7:0)	R/W	8
010	0x880 0004	Transfer Count Middle (15:8)	R/W	8
010	0x880 0008	FIFO Data	R/W	8
010	0x880 000c	Command	R/W	8
010	0x880 0010	Status	R	8
010	0x880 0010	Select-Reselect Bus ID	W	8
010	0x880 0014	Interrupt	R	8
010	0x880 0014	Select-Reselect Time-Out	W	8
010	0x880 0018	Sequence Step	R	8
010	0x880 0018	Synchronous Transfer Period	W	8
010	0x880 001c	FIFO Flags	R	8
010	0x880 001c	Synchronous Offset	W	8
010	0x880 0020	Configuration #1	R/W	8
010	0x880 0024	Clock Conversion Factor	W	8
010	0x880 0028	Test (Chip Test Use Only)	W	8
010	0x880 002c	Configuration #2	R/W	8
010	0x880 0030	Configuration #3	R/W	8
010	0x880 0038	Transfer Count High (23:16)	R/W	8

1. (chip_sel,sb_pa_(w,x,y)) = sb_pa(27,26,23,22) in a typical system.

Ethernet Block

The ENET block is based on the NCR92C990 ASF which is a superset of (and fully backwards compatible with) the AM7990 previously found on SPARCstations.

Differences

The only differences between the NCR92C990 and the AM7990 are:

- Programmable Inter Packet Gap (IPG). The NCR92C990 allows one to program the Transmit after Transmit (Tx-Tx) or Transmit after Receive (Rx-Tx) IPG time within the range of 9.6 μ sec (the Ethernet spec minimum IPG) to 22.4 μsec.

  This feature can be accessed via the upper bits of CSR3, as shown below:

CSR3 Bit	Description
15	Enable programmable IPG (default is 0, not programmable)
14-12	Rx-Tx IPG value: (default=110 or 20.8 μsec)
11-9	Tx-Tx IPG (default=000 or 9.6 μsec)
8-0	As normally defined in AM7990

  NOTE:
  - The formula for calculating the IPG value is [9.6 + 1.6*(3 bit IPG #)] μsec
  - The default values chosen to closely mimic the operation of the AM7990.

  The programmable IPG time assumes its default value should ANY of the following occur:

- Ethernet hard reset (either as a result of an SBus reset or the E_CSR E_RESET bit of the DMA2).
- The CSR0 STOP bit is set.
- The CSR0 INIT bit is set.
- The CSR3 Enable programmable IPG is reset to 0.

Software drivers should set CSR3 right after the last INIT, while waiting for the IDON interrupt. It is recommended that the Enable, Rx-Tx IPG and Tx-Tx IPG fields be ORed into all CSR3 writes.

- The NCR92C990 core used in the 89C100 differs from both the AM7990 and the stand-alone NCR92C990 core with respect to the memory error (MERR) time-out value. The description for bit 11 (ME) in the Control/Status Register 0 tables shows that READYb_IN must be received within 25.6us after asserting DAL_OUT(15:0). This value has been extended to 102.4us (4X) to avoid memory errors in high latency systems. This feature helps to avoid unneeded reinitializations of the NCR92C990 during periods of high system activity.

  Refer to "NCR92C990 Ethernet Core" for details.

Ethernet Block Diagram

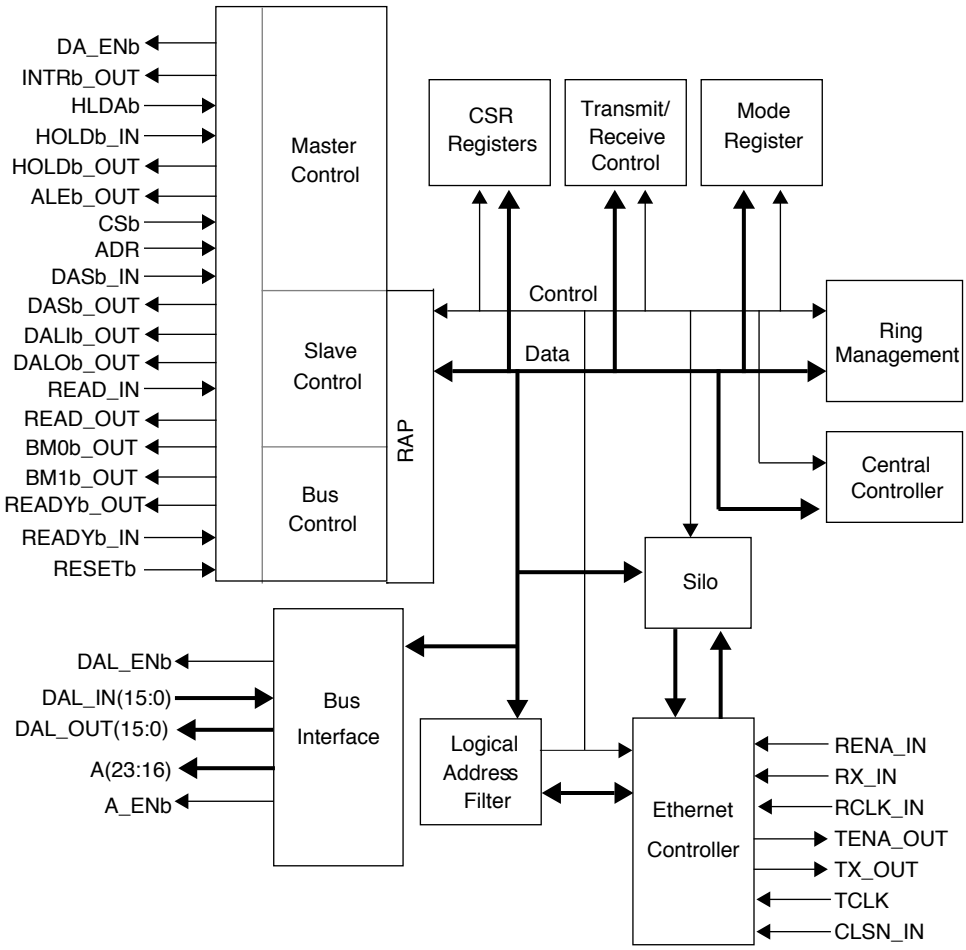


Figure 2-6 Ethernet Block Diagram

Ethernet-Level Address Map

Table 2-10 NCR92C990 Registers

sb_pa_(w,x,y)[1]	sb_pa(27:0)	Register Accessed	Type	Size
	0x8c0 0000 -> 0x8c0 0003	Ethernet Controller Registers		
011	0x8c0 0000	Register Data Port (RDP)	R/W	16
011	0x8c0 0002	Register Address Port (RAP)	R/W	16

1. (chip_sel,sb_pa_(w,x,y)) = sb_pa(27,26,23,22) for the mapping shown.

Test Block

The 89C100 contains an IEEE JTAG1149.1 compliant test controller and boundary scan architecture. All mandatory instructions are supported, and this document contains the chip specific boundary scan information. The 89C100 also contains internal test logic and reserved instructions. The basic description of this logic appears below but is not supported.

This section describes the goals and implementation of the testability features implemented in the 89C100. These features have been incorporated to provide a structured test approach to both device fabrication testing and board-level testing and debug.

JTAG Scan Access

The goals for the 89C100 testability are to provide for high stuck at fault coverage at both the IC and board level. This is provided by the incorporation of an IEEE 1149.1 (JTAG) compatible TAP controller and boundary scan, which in conjunction with modular broadside access modes provides access to each of the major functional blocks on the I/O chips through either full scan (in the case of the DMA2 block) or boundary scan (in the case of the NCR ASFs). These ASFs are tested during device fabrication by a full broadside pin mode that provides direct access to all ports of each ASF from the device pins. This allows standardized test patterns to be applied directly to each ASF without the need for additional high fault coverage patterns for these blocks. At the board-level, the JTAG compatible boundary scan provides for complete access to PCB interconnect, including die to package bonding.

Block Access Modes

Diagnostic multiplexing between the pad ring and the internal ASFs is configurable into four different modes: Normal Mode, in which the device operates as required in the system; TBLK1 Mode, for scanned logic, in which all the ports to the DMA2 logic are accessible via scannable elements. In addition, the internal scan chain of the block is connected in series with the boundary scan chain, and the partition scan chain (if one is required) to form a complete scan path for access to all state and primary inputs of the block. TBLK2 and TBLK3, for NCR designed logic, in which each block is presented to the pins of the device as if it were a stand-alone device.

Tristate Pin Function

All output pins of the device are tristate-able, controlled by elements in the boundary scan chain, to support manufacturing system test. At power-up and in normal operation of the system this function is disabled by the TRSTB JTAG pin being held in the active low state.

Block Diagnostic Modes

TBLK1 (Internal Scan) Diagnostic Mode

Figure 2-1 illustrates the operation of the TBLK1 diagnostic mode. In this mode, the test logic is configured to connect every primary input to the Q-output of a scannable flip-flop and every primary output to the D-input of a scannable flip-flop. In addition, every flip-flop inside the block is configured into a single scan chain, known as the internal, or "iscan" chain.

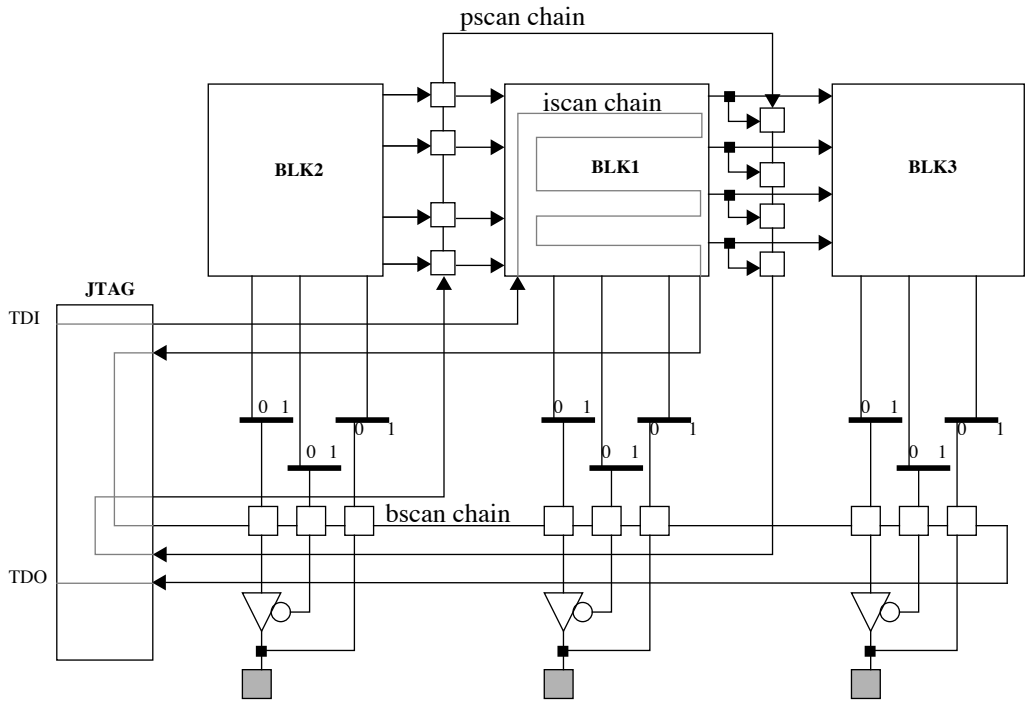


Figure 2-7 TBLK1 (Internal Scan) Diagnostic Mode

TBLK2/TBLK3 Diagnostic Mode

Figure 2-2 illustrates the operation of the TBLK2(TBLK3) diagnostic mode. In these modes the test logic is configured to connect internal inputs and outputs to BLK2 (BLK3) to pins normally assigned to BLK1 or BLK3(BLK2). Since these blocks are non-scannable, the only function of the JTAG controller in this mode is to configure the multiplexor logic into this mode. Hence the scan datapath is placed in BYPASS mode.

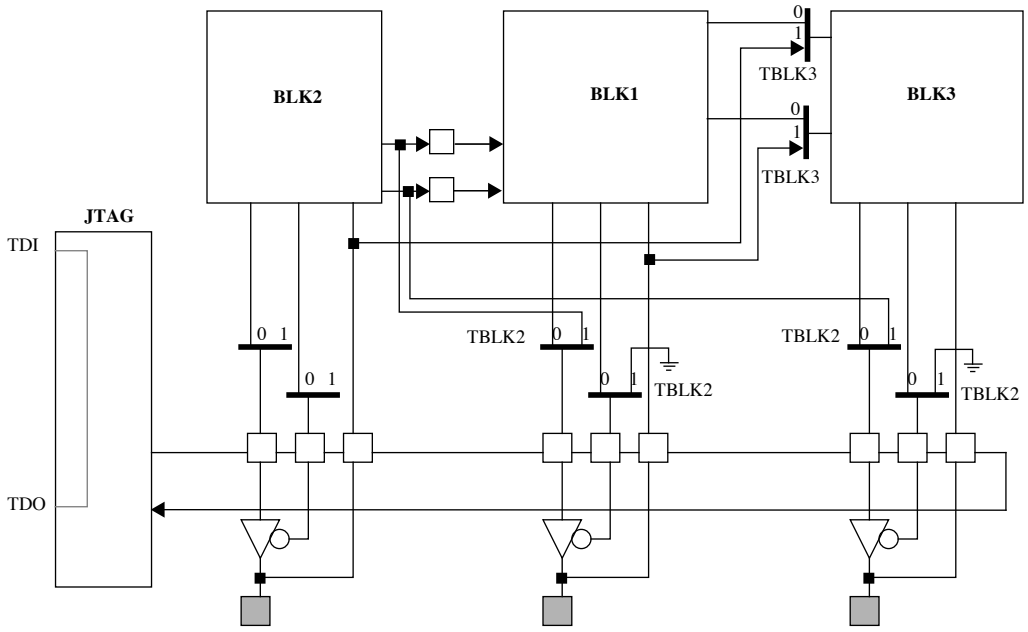


Figure 2-8 TBLK2/TBLK3 Diagnostic Mode

Outputs of the block that normally connect to BLK1 are multiplexed into the chip outputs of the other blocks, configured by the TBLK2(TBLK3) mode signal. Inputs to BLK2 (BLK3) are multiplexed with inputs from the other blocks. Figure 2-2 shows how the outputs of BLK2 and the inputs of BLK3 are configured.

Other JTAG test modes (TBLK2_BS and TBLK3_BS) are provided that operate identically except that the scan data path is configured to pass through the boundary chain. This allows application of the broadside test vectors to the blocks using the boundary chain to drive primary inputs and sample primary outputs in a pseudo-static manner, i.e. it does not directly support complex edge relationships between inputs. Instead these vectors must be "exploded" into multiple boundary scan vectors.

JTAG Controller

The JTAG controller contains the following elements:

- NCR Tap controller
- Scan Datapath including instruction register, bypass register and ID register
- Clock control register and state machine

The following figure shows a simplified block diagramof the JTAG controller. It has been partitioned into two main functional areas: Scan Datapath and Scan Control Logic.

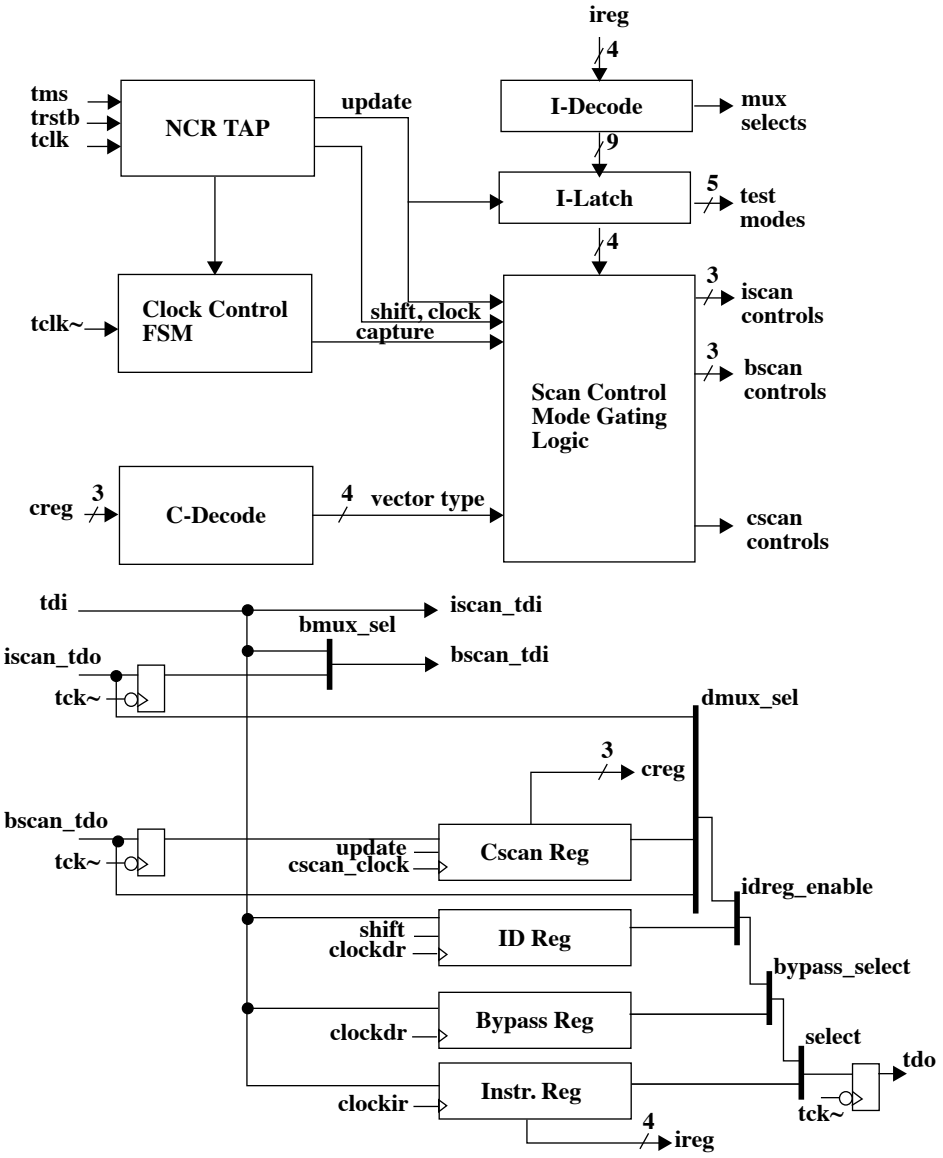


Figure 2-9 JTAG Controller Block Diagram

The NCR tap controller is a standard cell implementation of a reference 1149.1 tap state machine[1]. It is connected directly to the test access port on the 89C100 (TCK, TMS, TRSTB) and generates the basic scan controls (clock_dr, clock_ir, reset_l, select, shift_dr, shift_ir, update_dr, update_dr) which are used to control the scan architecture.

The NCR TAP implementation has been modified slightly to also make available the TAP state for use by supplemental state machines. The NCR state machine implements the reference state diagram described by the 1149.1 specification[2]. The state coding is shown Table 2-12.

1. IEEE Std. 1149.1-1990 chapter 5.
2. IEEE Std. 1149.1-1990 page 5-1.

Table 2-11 State Assignments for NCR TAP Controller

Controller State	State[3:0]
Exit2-DR	0
Exit1-DR	1
Shift-DR	2
Pause-DR	3
Select-IR-Scan	4
Update-DR	5
Capture-DR	6
Select-DR-Scan	7
Exit2-IR	8
Exit1-IR	9
Shift-IR	A
Pause-IR	B
Run-Test/Idle	C
Update-IR	D
Capture-IR	E
Test-Logic-Reset	F

The instruction register for the 89C100 is a 4- bit register comprised of simple scannable elements. When the TAP state machine issues a reset signal this register is initialized to the IDCODE (1110) instruction. The parallel inputs of the instruction register are not used to load design-specific information and are tied-off to logic 0.

The 4-bit output of the instruction register is followed by an instruction decode stage which decodes up to 16 unique instructions. Not all of these are used by the 89C100 but are given mnemonics for completeness.

Table 2-2-12 lists these mnemonics and the instruction value that corresponds to

them:

Table 2-12 Decoded JTAG Instructions

Value	Mnemonic	Description
0000[1]	EXTEST	Boundary scan board interconnect test.
0001	SAMPLE	Boundary scan sample/preload.
0010	TBLK1	BLK1 ATPG scan test mode (Internal+-Boundary+Clock chains).
0011	TBLK2	BLK2 broadside test mode (Bypass).
0100	TBLK3	BLK3 broadside test mode (Bypass).
0101	RESERVED	—
0110	PSCAN	Reserved for partition scan (if implemented, otherwise Bypass).
0111	INTEST	Boundary scan capture of internal I/O.
1000	TBLK2_BS	BLK2 boundary scan test mode.
1001	TBLK3_BS	BLK3 boundary scan test mode.
1011	TPSCAN	Reserved for BLK1 tester partition scan mode (if implemented, otherwise Bypass). Other BLK1 pins controlled by broadside tester.
1100	BPSCAN	Reserved for BLK1 boundary partition scan mode (if implemented, otherwise Bypass). Other BLK1 pins controlled by boundary scan.
1101	ZMODE0	General purpose test mode.
1110	IDCODE	Device ID register.
1111[1]	BYPASS	Bypass mode.

1. Required instruction.

The scan controls decoded by these instructions configure the scan datapath, the test multiplexors and control the clocks and pseudo clocks for the test mode in progress.

Instruction Decode

The I-Decode logic converts the 4-bit instruction register contents into decoded signals that control mux selection in the scan datapath and test mode configuration in the ASFs. Nine of these signals are latched by the I-latch to provide glitch free values on these signals which are updated during the IR-Update state.

Clock Control FSM

The clock control finite state machine monitors the state output from the NCR TAP controller and determines when it is necessary to insert the capture clock and/or pseudo clocks required to support ATPG stimulus application to BLK1. The clock gating is designed such that the boundary clock is guaranteed to be asserted at all elements of the boundary scan chain before it is applied to either the clock or pseudo clock (set/reset) inputs to the BLK1 internals. This requirement is present due to the fact that ATPG vectors have an assumed order in which stimulus is applied to the circuit and state or primary outputs are captured. The clock control state machine in the 89C100 has been verified to support the requirements of TestScan ATPG from Cadence Design Systems, Inc. although it may function equally well with other ATPG systems.

The assumed sequence of operations required for ATPG pattern application is:

1. Stimulate pins - boundary and pscan chains shift/update sequence.
2. Stimulate shift register/latches - internal scan chain shift in.
3. Measure pins - boundary and pscan chain capture sequence.
4. Pulse clocks/pseudo clocks - internal chain clock/set/reset.
5. Measure shift register/latches - internal scan chain shift out.

The Clock Control FSM has been designed to support this event ordering in a single continuous shift-update-capture-shift sequence. In TBLK1 mode the scan chains within the 89C100 are concatenated into a single chain containing internal, boundary and clock control scan chains. Hence after an initial shift-update sequence, the requirements of (1) and (2) have been met. The Capture-DR state is then used to measure the state of the primary outputs of BLK1 by issuing a clock to the boundary with the shift control not asserted. A delayed version of the clock (or update pulse in the case of the pseudo clocks) is then used to apply clock, set or reset to the internal scan chain to implement the internal chain capture. This occurs only when indicated by the value of the “capture” output from the clock control state machine.

Clock Control Register

The other three bit positions in the clock control scan chain are transferred to the clock control register during a DR-update sequence, where they are decoded by the C-Decode logic to specify which vector class the following capture sequence belongs to out of the following categories:

1. Shift only, no capture.
2. Capture scan chain, (i.e. shift high during capture clock).
3. Normal clocked vector.
4. Set vector, no clock.
5. Reset vector, no clock.

Since the last two categories are only required when the logic under test contains asynchronous sets or resets, they are not required for the 89C100.

Mode Gating Logic

The decoded vector type information is combined with the clock control FSM information and the primary scan controls from the NCR TAP controller and instruction register decodes to generate control signals for each of the four scan chains with the 89C100: iscan, bscan, pscan (if present) or cscan. These signals are buffered and distributed throughout the device to the various chain elements. Since the 89C100 does not require a partition scan chain for its final implementation, these controls have been deleted.

Scan Datapath

The scan datapath within the JTAG Controller contains the chain configuration logic, implemented as a series of multiplexors; inter-chain flops to guarantee hold margins; the Cscan register; JTAG compliant ID, BYPASS and IR shift registers and the TDO output multiplexors and flop. This datapath, like the external scan chains and test logic is controlled by the scan control logic described above. The only variation from a more conventional IEEE 1149.1 implementation is the ability to configure the scan chain into various different modes based on the instruction type. The use of the hold flops, clocked by TCK~ is simply an implementation detail to reduce the effects of clock skew between the separate scan chains.

The 89C100's scan datapath does not include a partition scan chain, as in its final implementation this functionality has been incorporated into the internal, or "iscan" chain to facilitate physical implementation of the device. The elements of the embedded partition scan chain are therefore controlled by the same datapath controls as the existing iscan chain elements.

Table 2-14 lists the lengths of the various scan chains that comprise the 89C100's scan datapath.

Table 2-13 89C100 JTAG Chain Lengths

Chain Name	Number of Elements
BYPASS	1
I.D.	32
Instruction Register	4
Internal	893
Boundary	209
ATPG	1105

Performance

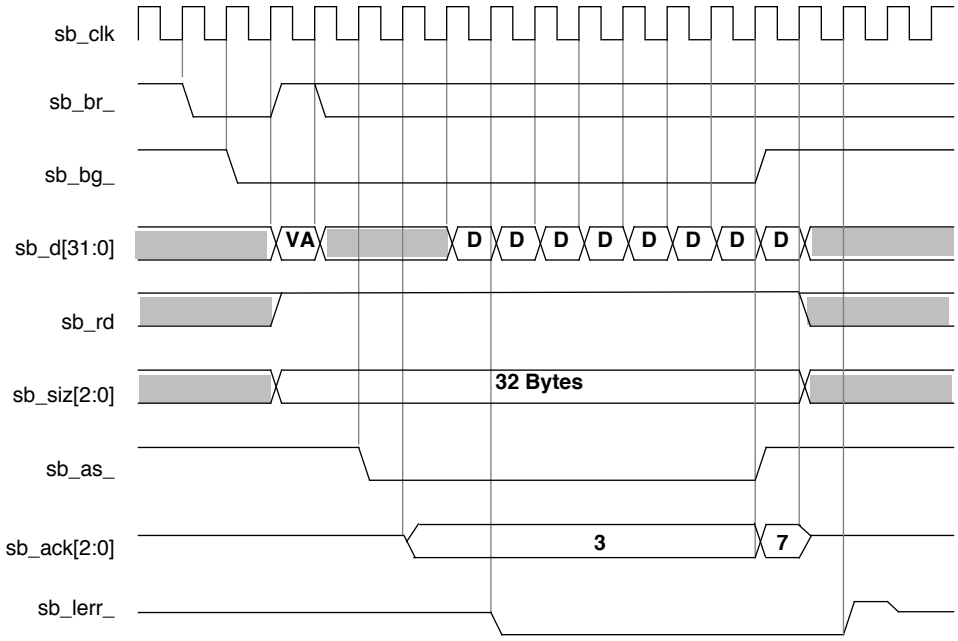
The design as implemented in NCR's VS700H 0.95um (drawn) standard cell library has been verified to operate at a 5MHz scan rate.

The JTAG controller occupies approximately 700 gates, and the scan overhead for the simple multiplexed flop scan element that it supports is estimated at about 10% from a gate count perspective, 5% in total area overhead.

Functional Timing Diagrams

These timing diagrams illustrate a DMA access by the 89C100 on the SBus as well as all the common slave accesses to the 89C100 address ports. Optimal translation time (1 cycle) is assumed for DMA.

SBus DMA Burst Read (1 Word/Clock)



(Data flow from memory to the DMA2)
For other possible SBus cycles, see the SBus Specification; this is just one example.

Figure 2-10 SBus DMA Burst Read (1 Word/Clock)

DMA2 ENET and SCSI Register Accesses

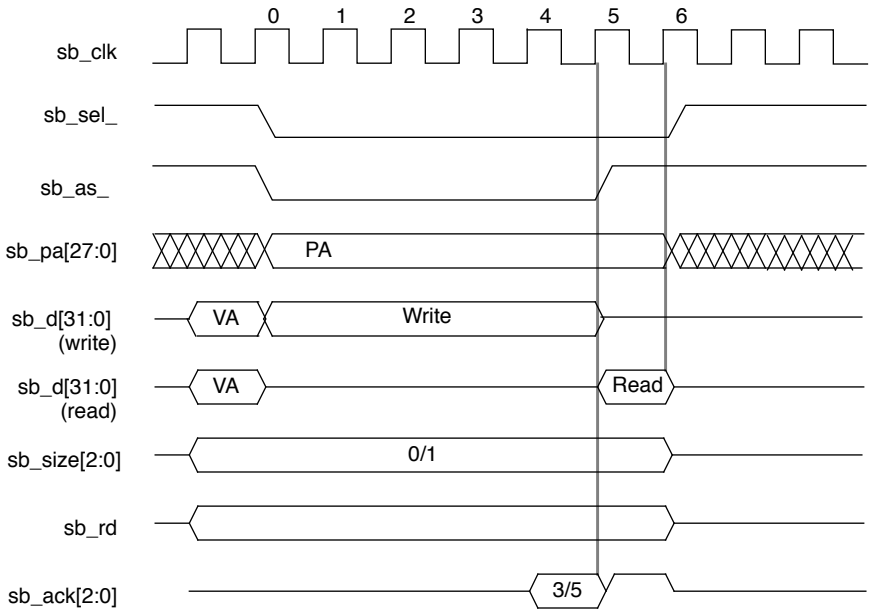


Figure 2-11 DMA2 ENET and SCSI Register Accesses

DMA2 Parallel Port Register Accesses

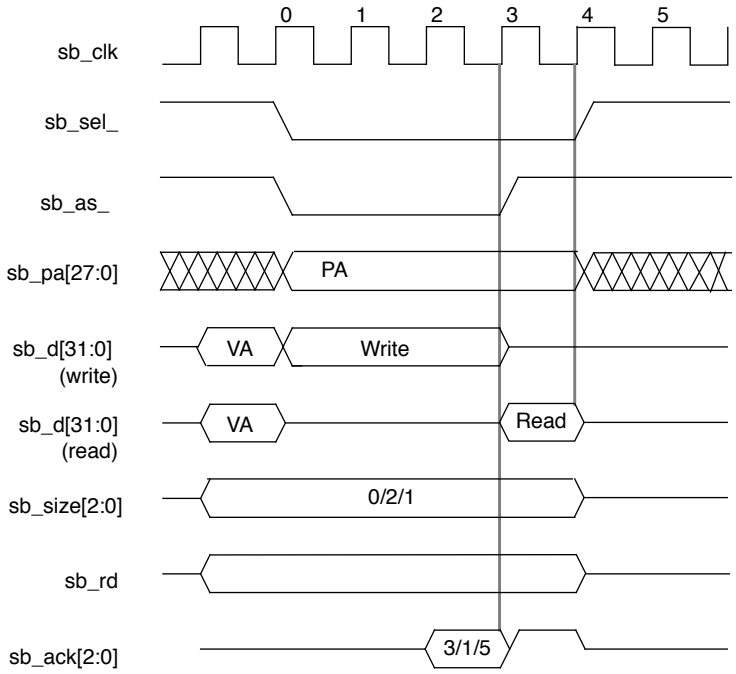


Figure 2-12 DMA2 Parallel Port Register Accesses

ENET Controller Register Accesses

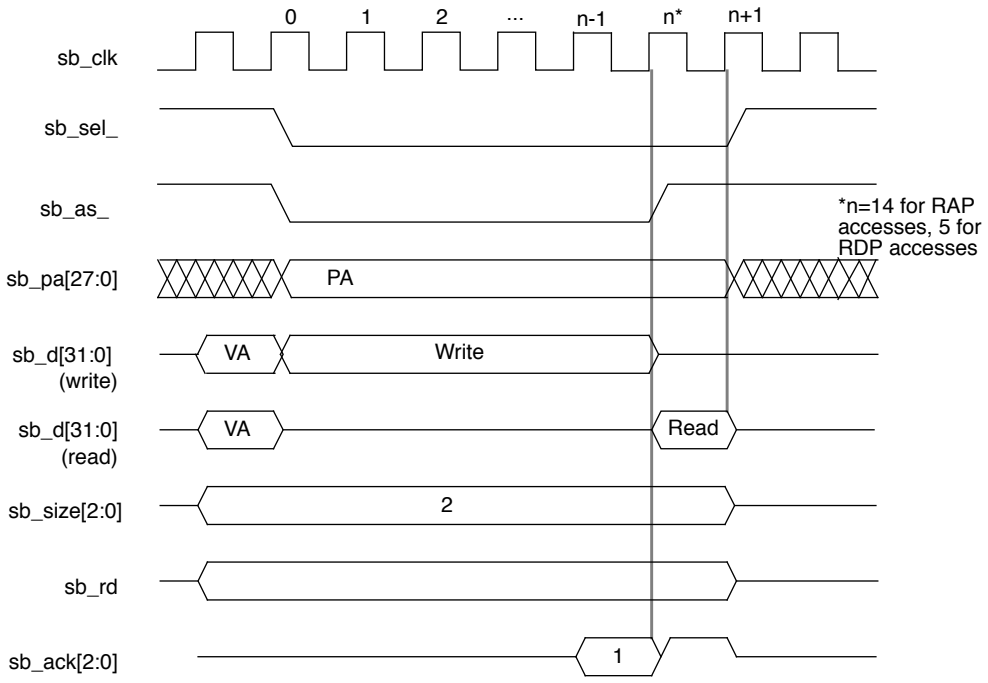


Figure 2-13 ENET Controller Register Accesses

SCSI Controller Register Access

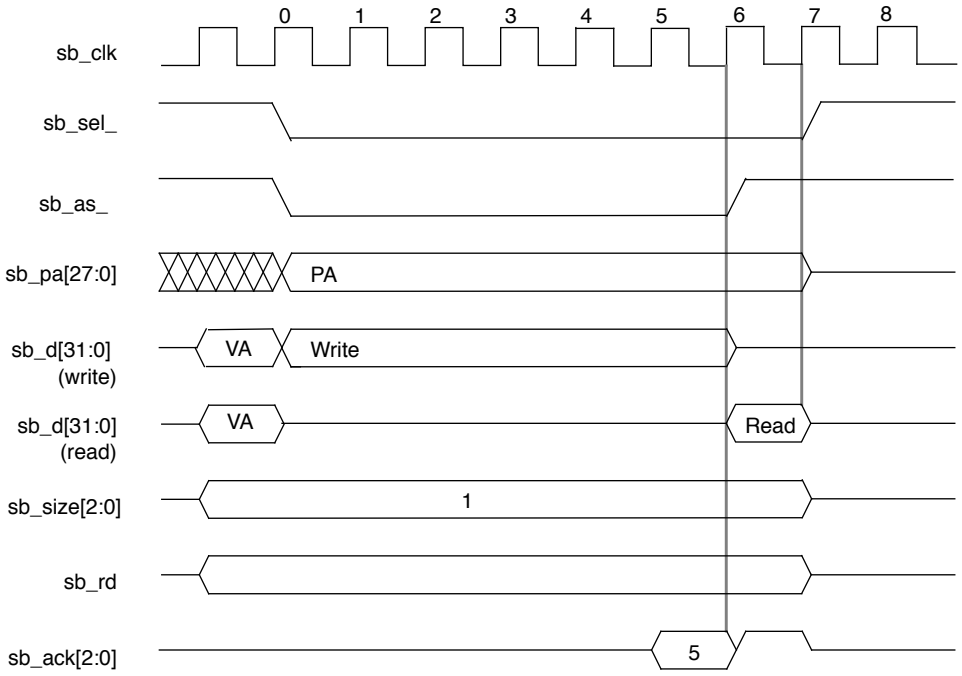


Figure 2-14 SCSI Controller Register Accesses

External ID PROM Read Access

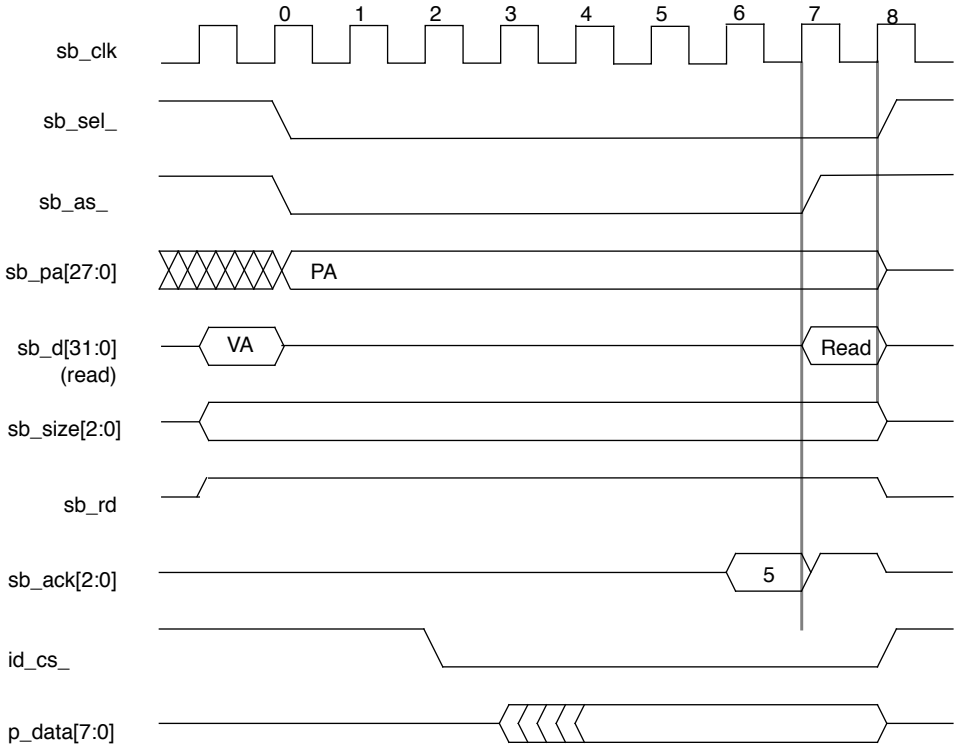


Figure 2-15 External ID PROM Read Access

Electrical Considerations

This section defines the following electrical specifications for the 89C100:

- Absolute and recommended operating conditions
- DC characteristics
- AC characteristics
- Power consumption

The 89C100 is implemented in NCR's VS700H process, and normal handling precautions required by all MOS devices must be observed. Regardless of the fact that all inputs and outputs are protected against ESD damage by internal protection structures, the device can be degraded or destroyed by exposure to high electrostatic fields.

Absolute Maximum Ratings

The following section details the absolute maximumratings of the 89C100 chip. Operation of the device at values in excess of those listed here will result in degradation or destruction of the device and should be avoided. This table does not imply that functional operation at conditions above those listed in the "Recommended Operating Conditions" is possible. This is a stress rating and operation of a device at or above this rating may cause failure or affect reliability.

Table 2-14 Absolute Maximum Operating Conditions

Name	Symbol	Min	Max	Units
Supply Voltage	V_{dd}	-0.5	+7	Volts
Input, Output Voltage	V_{im}	-0.5	V_{dd} + 0.5	Volts
Current Drain Vdd and Vss pins	I_i		100	mA
Lead Temperature (less than 10 second soldering)	T_l		250	°C
Operating Temperature	T_j	0	70	°C
Storage Temperature	T_s	-55	150	°C

Recommended Operating Conditions

The following section details the recommended DC operating conditions for the 89C100 chip:

Table 2-15 Recommended Operating Conditions

Name	Symbol	Min	Nom	Max	Units
Supply Voltage	Vdd	4.75	5.0	5.25	Volts
Operating Free-Air Temperature	Ta	0	25	70	°C

DC Characteristics

This table specifies the DC characteristics of the 89C100 chip over the range of the recommended operating conditions.

Table 2-16 DC Characteristics

Name	Symbol	Min	Nom	Max	Units
TTL Input Receiver					
High Level Input Voltage	V_{ih}	2.0			Volts
Logic Low Input Voltage	V_{il}			0.8	Volts
DS1216 Schmitt Input Receiver					
High Level Input Voltage	V_{ih}	1.9	1.6		Volts
Logic Low Input Voltage	Vil		1.2	0.9	Volts
DS1218 Schmitt Input Receiver					
High Level Input Voltage	V_{ih}	2.1	1.8		Volts
Logic Low Input Voltage	V_{il}		1.2	0.9	Volts
DS1238 Schmitt Input Receiver					
High Level Input Voltage	V_{ih}	4.1	3.8		Volts
Logic Low Input Voltage	V_{il}		1.2	0.9	Volts
Minimum high-level source current, V_{oh} = 2.4 V					
2 mA buffer	I_{oh}	2.0			mA
4mA buffer		4.0			
8mA buffer		8.0			
16 mA buffer		16.0			
24 mA buffer		24.0			
48mA buffer		n/a			
Minimum low-level sink current, V_{ol} = 0.4 V					
2 mA buffer	I_{ol}	2.0			mA
4mA buffer		4.0			
8mA buffer		8.0			
16 mA buffer		16.0			
24 mA buffer		24.0			
48mA buffer		48.0			
SCSIPAD (V_{ol} = 0.5 V)		48.0			
SCSIPADF (V_{ol} = 0.5 V)		48.0			

Table 2-16 DC Characteristics

Name	Symbol	Min	Nom	Max	Units
Input Leakage Current	I_{in}			±10	µA
Tristate Output Leakage Current	I_{oz}			±10	µA
High Level Output Voltage	V_{oh}	4.4	4.5		Volts
Low Level Output Voltage	V_{ol}		0.0	0.1	Volts
Input Capacitance	Ci		6		pF
Output Capacitance	Co		6		pF
Bidirectional Pin Capacitance	Cb		6		pF
SCSI Pin Capacitance				10	pF

AC Characteristics

The following table lists the 89C100 AC characteristics specification:

Table 2-17 89C100 AC Characteristics

Number	Description	Conditions	Min	Max	Units
SBus Timing					
1	Clock Period		40.0	60.0	ns
2	Clock High		17.0		ns
3	Clock Low		17.0		ns
4	Hold wrt CLK Rising		0.0		ns
5	Setup to CLK Rising		15.0		ns
6	Hold wrt CLK Rising	See Note 1	1.0		ns
7	Hold wrt CLK Rising		0.0		ns
8	CLK Rising to Output Valid	160 pF load	2.5	22.5	ns
9	CLK Rising to Output Invalid	160 pF load	2.5	20.0	ns
Parallel Port Timing					
10	CLK to p_d_strb	75 pF		35	ns
11	p_d_strb nom. width	DSW=0,1,2,3	3		sb.clk periods
12	p_data valid to p_d_strb assert	75 pF	5		ns
13	p_data valid (nominal)	DSS=0,DSN=3	6		sb_clk periods
14	p_ack, p_bsy setup to clk		5		ns

Table 2-17 89C100 AC Characteristics (Continued)

Number	Description	Conditions	Min	Max	Units
15	p-ack,p_bsy input pulse width		3		sb_clk periods
16	p_d_strb setup to clk		5		ns
17	p_d_strb input pulse width		3		sb_clk periods
18	p_data setup to p_d_strb		36		ns
19	p_data input hold from p_d_strb		4		sb_clk periods
20	p_d_strb to p_bsy valid	75 pF	2	3+26 ns	sb_clk periods
21	CLK to p_ack, p_bsy	75 pF		40	ns
22	p_ack, p_bsy nominal pulse width	75 pF	3		sb_clk periods
23	CLK to output	75 pF		35	ns
SCSI Timing					
24	Clock period (t_{CP})		25	83.3	ns
25	Synchronization latency		t_{CL}	t_{CL}+t_{CP}	ns
With FASTCLK bit reset					
26	Clock frequency, asynchronous	See Note 2	12*	25	MHz
27	Clock frequency, synchronous	See Note 2	20*	25	MHz
28	Clock high		14.58	0.65*t_{CP}	ns
29	Clock low (t_{CL})		14.58	0.65*t_{CP}	ns
With FASTCLK bit set					
26	Clock frequency, asynchronous	See Note 2	20*	40	MHz
27	Clock frequency, synchronous	See Note 2	38*	40	MHz
28	Clock high		0.40*t_{CP}	0.60*t_{CP}	ns
29	Clock low (t_{CL})		0.40*t_{CP}	0.60*t_{CP}	ns
Asynchronous SCSI					
30	Data setup to scsi_ack_/ scsi_req_ low		60		ns
31	Data hold from scsi_req_ high/scsi_ack_ low	See Note 3	5		ns
32	scsi_ack_ low to scsi_req_ high			50	ns

Table 2-17 89C100 AC Characteristics (Continued)

Number	Description	Conditions	Min	Max	Units
33	scsi_ack_ high to scsi_req_ low (data already setup)	See Note 4		45	ns
34	scsi_req_ high to scsi_ack_ high			50	ns
35	scsi_req_ low to scsi_ack_ low (data already setup)	See Note 4		50	ns
36	Data setup to scsi_req_/ scsi_ack_ low		0		ns
37	Data hold from scsi_req_/ scsi_ack_ low			18	ns
Synchronous SCSI					
Normal SCSI					
38	Data setup to scsi_req_/ scsi_ack_ low		55		ns
39	Data hold from scsi_req_/ scsi_ack_ low		100		ns
40	scsi_req_/scsi_ack_ assertion period		90		ns
41	scsi_req_/scsi_ack_ negation period		90		ns
Fast SCSI					
38	Data setup to scsi_req_/ scsi_ack_ low		25		ns
39	Data hold from scsi_req_/ scsi_ack_ low		35		ns
40	scsi_req_/scsi_ack_ assertion period		30		ns
41	scsi_req_/scsi_ack_ negation period		30		ns
Synchronous SCSI Input Cycle					
42	Data setup to scsi_req_/ scsi_ack_ low		5		ns
43	Data hold from scsi_req_/ scsi_ack_ low		15		ns
44	scsi_req_ assertion period		27		ns
45	scsi_req_ negation period		20		ns
46	scsi_ack_ assertion period		20		ns
47	scsi_ack_ negation period		20		ns
Ethernet Timing					
48	enet_tclk period		99	101	ns

Table 2-17 89C100 AC Characteristics (Continued)

Number	Description	Conditions	Min	Max	Units
49	enet_tclk high pulse duration		45		ns
50	enet_tclk low pulse duration		45		ns
51	enet_tclk rise time			8	ns
52	enet_tclk fall time			8	ns
53	enet_tena propagation delay after rising edge of enet_tclk			25	ns
54	enet_tena hold time after enet_tclk rising		7		ns
55	enet_tx propagation delay after enet_tclk rising			32	ns
56	enet_tx hold time after enet_tclk rising		7		ns
57	enet_rclk period		85	118	ns
58	enet_rclk high pulse duration		38		ns
59	enet_rclk low pulse duration		38		ns
60	enet_rclk rise time			8	ns
61	enet_rclk fall time			8	ns
62	enet_rx data rise time			8	ns
63	enet_rx data fall time			8	ns
64	enet_rx data hold time from enet_rclkrising		5		ns
65	enet_rx data setup time to enet_rclkrising		40		ns
66	enet_rena low duration		120		ns
67	enet_clsn high duration		110		ns
68	enet_rena hold time after the rising edge of enet_rclk		1		ns
69	enet_rena defer before enet_tena		356		ns
70	enet_rena extended after enet_rclk last falling			275	ns

NOTE 1: This is the only violation of SBus Specification B.0. No known implementation to date provides less than 1.0 ns hold time on these signals.

NOTE 2: These minimum numbers required to comply with ANSI SCSI specification. For Synchronous SCSI data transfers and FASTCLK enabled, the clock inputs must also meet the following requirements: $2*t_{CP}+t_{CL}>97.92$ ns and $2t_{CP}+t_{CH}>97.92$ ns

NOTE 3: FIFO is not empty.

NOTE 4: FIFO is not full.

AC Timing Diagrams

SBus Input Signals

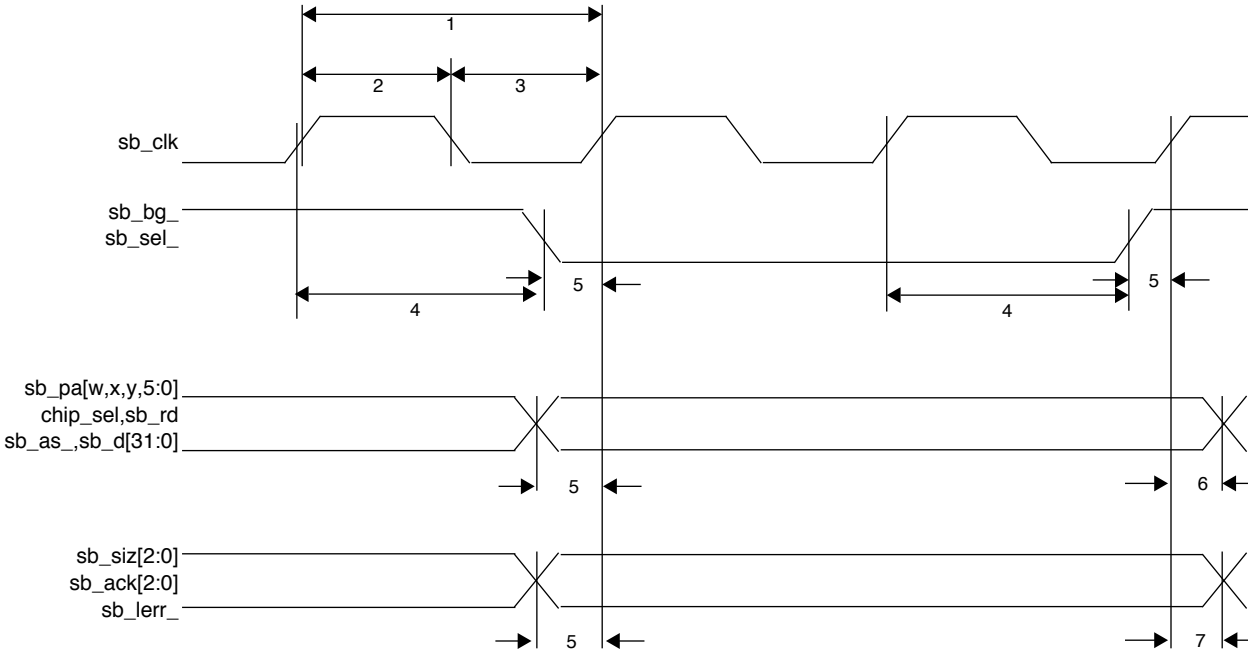


Figure 2-16 SBus Input Signals

SBus Output Signals

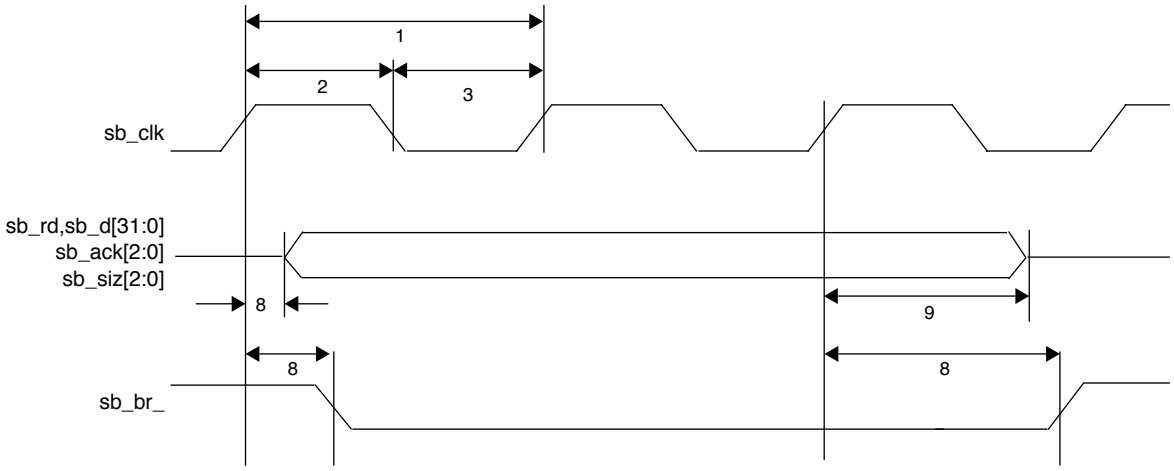


Figure 2-17 SBus Output Signal

Parallel Port Output Timing

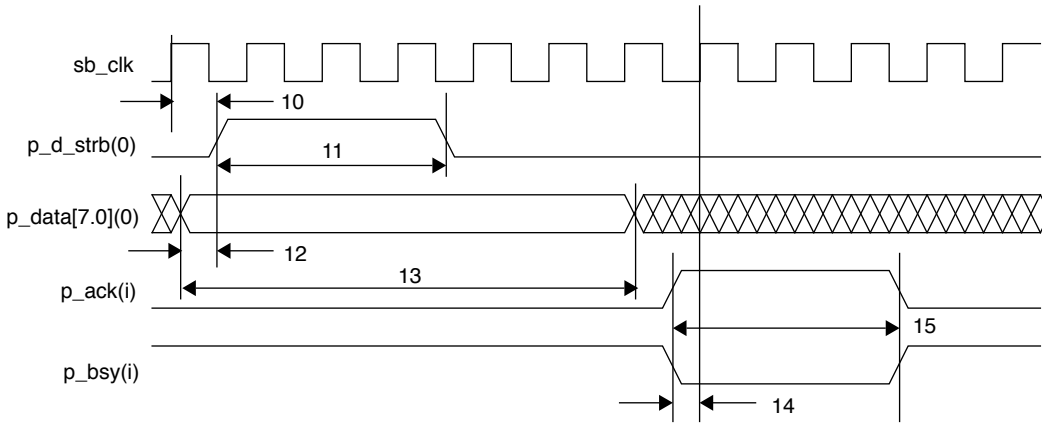


Figure 2-18 Parallel Port Output Timing

Parallel Port Input Timing

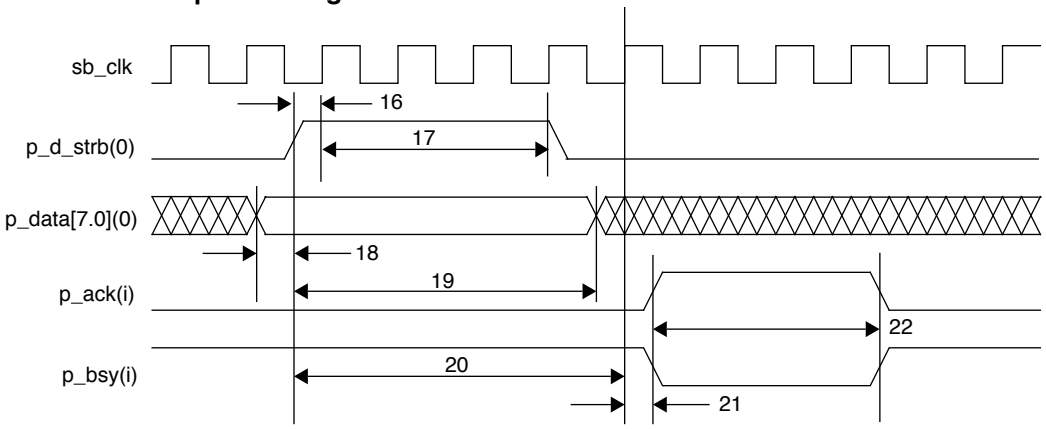


Figure 2-19 Parallel Port Input Timing

Parallel Port, Other Timing

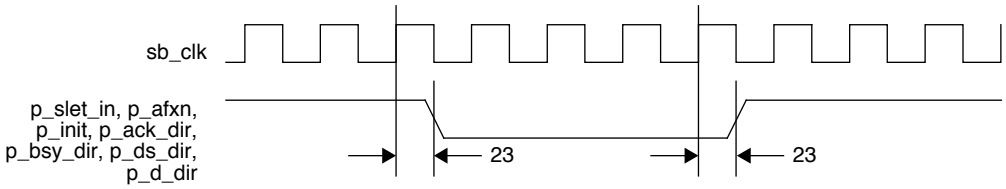


Figure 2-20 Parallel Port, Other Timing

SCSI Clock

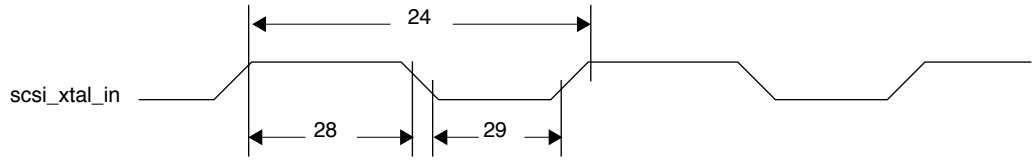


Figure 2-21 SCSI Clock

SCSI Asynchronous Output

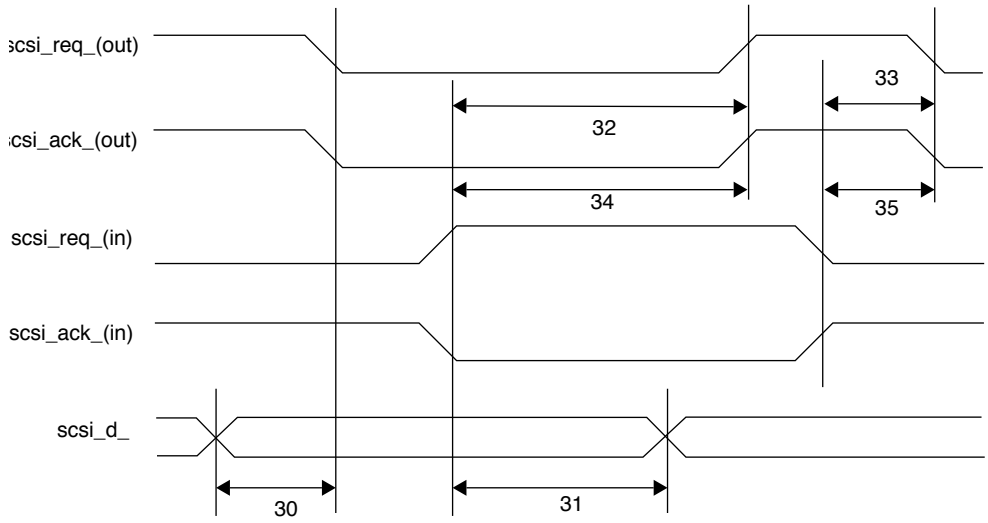


Figure 2-22 SCSI Asynchronous Output

SCSI Asynchronous Input

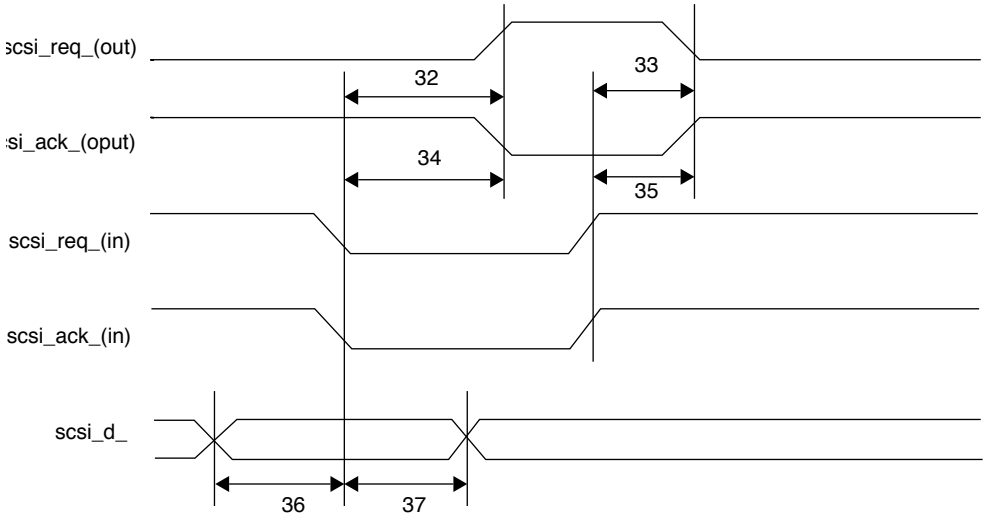


Figure 2-23 SCSI Asynchronous Input

SCSI Synchronous Output

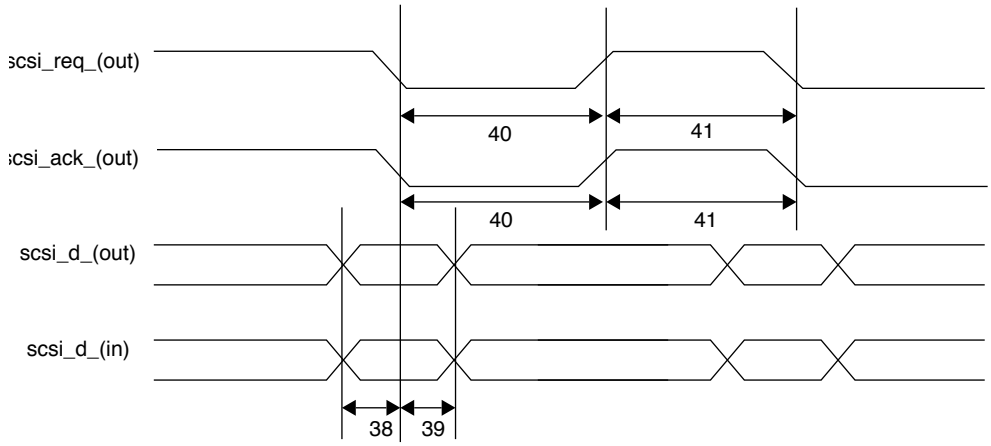


Figure 2-24 SCSI Synchronous Output

SCSI Synchronous Input

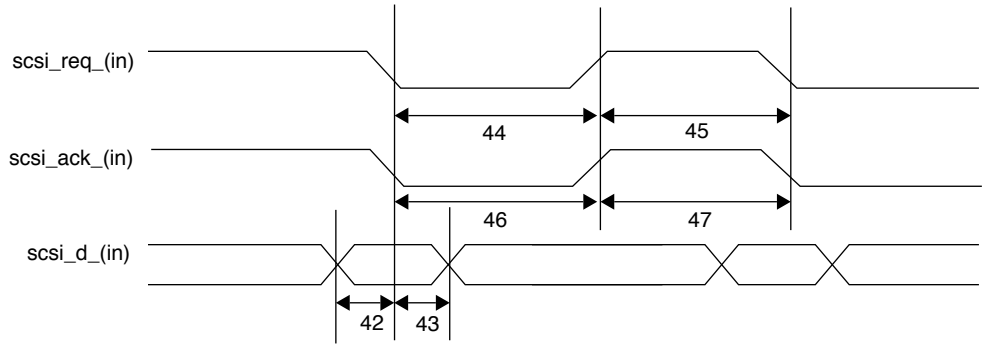


Figure 2-25 SCSI Synchronous Input

Ethernet Transmit/Receive Timing

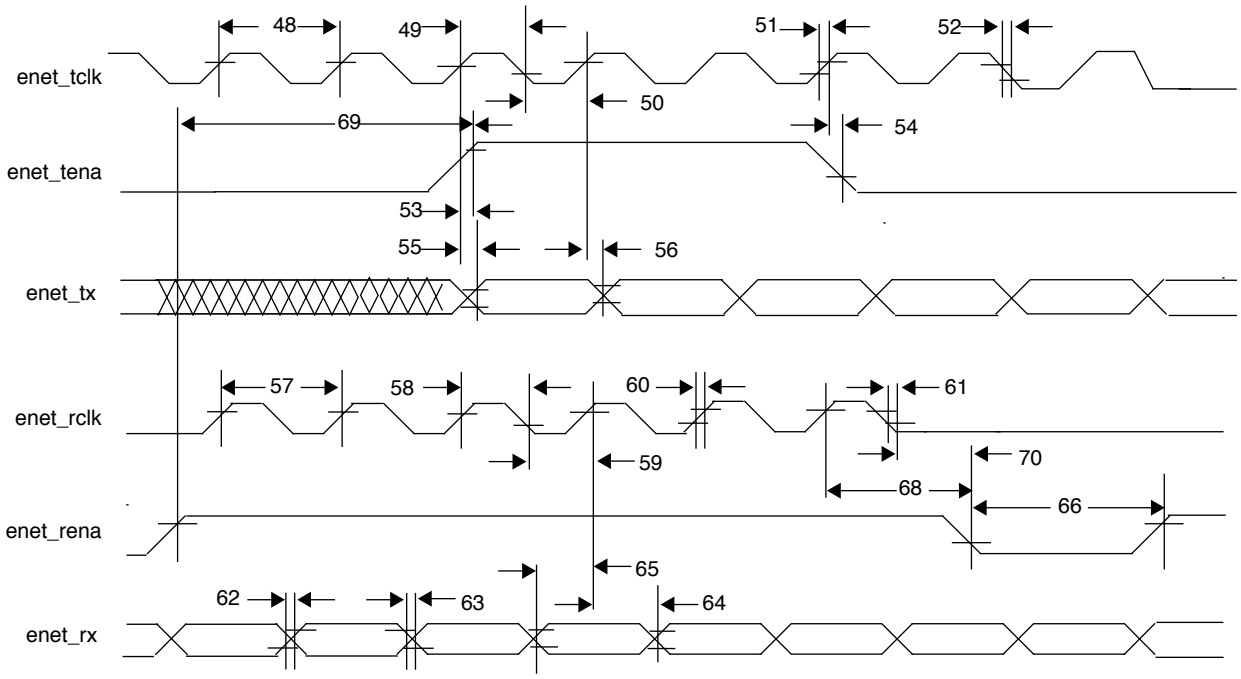


Figure 2-26 Ethernet Transmit/receive timing

Ethernet Collision Timing

Figure 2-27 Ethernet Collision Timing

Power Consumption

The 89C100 power consumption depends on SBus clock frequency, SBus and other output loading, and the workload. Power measurements are given for maximum loading (every ASF/functional block running in a manner to maximize power consumption) of the device. These measurements were taken over the entire operating ranges of voltage and temperature. The typical number reflects the average power consumed by the device under these conditions and the maximum number reflects the high limit of power that the part may consume in operation. Note that in normal system operation, the power consumption should fall at or below the typical number given here.

Table 2-18 Power Consumption

SBus Freq	Typical power	Maximum power	Units
25 MHz	750	1400	mW

The 89C100 is packaged in a 160-pin PQFP package, and uses a custom copper lead-frame to enhance thermal performance. The package thermal parameters are:

Table 2-19 Package Thermal Parameters (Still Air)

Θja	Units
24	°C/W

The 89C100 AC characteristics are given at 70°C junction temperature. By using the package characteristics and the power consumption numbers, one can get a rough idea of the allowable operating environments. Operation at junction temperatures in excess of 70°C is not recommended for performance reasons (the critical timing paths will not meet 25 MHz SBus specifications above this temperature). Operation at junction temperatures above 125° C is not recommended at any time, as it will cause reliability problems.

Packaging Information

The 89C105 chip is a standard cell design, based on the NCR VS700H technology (0.95 micron drawn, 0.7 effective).

Packaging Identification

The 89C105 is packaged in a 160 pin Plastic Quad Flat Pack (PQFP), with the following marking (the last line will be filled in with wafer lot and date code information):

Figure 2-28 Packaging Identification

Mechanical Packaging Specification

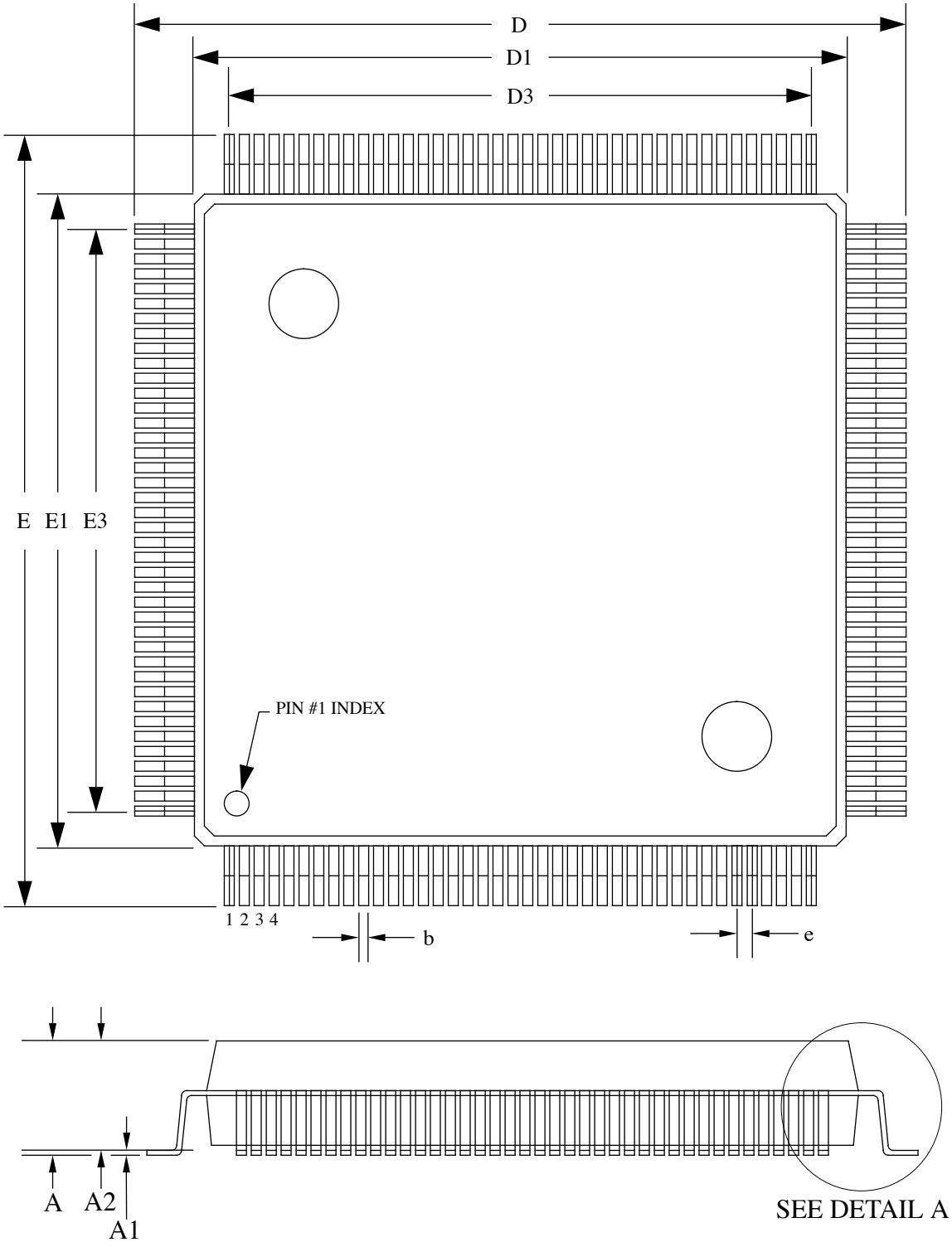


Figure 2-29 Mechanical Packaging Specification

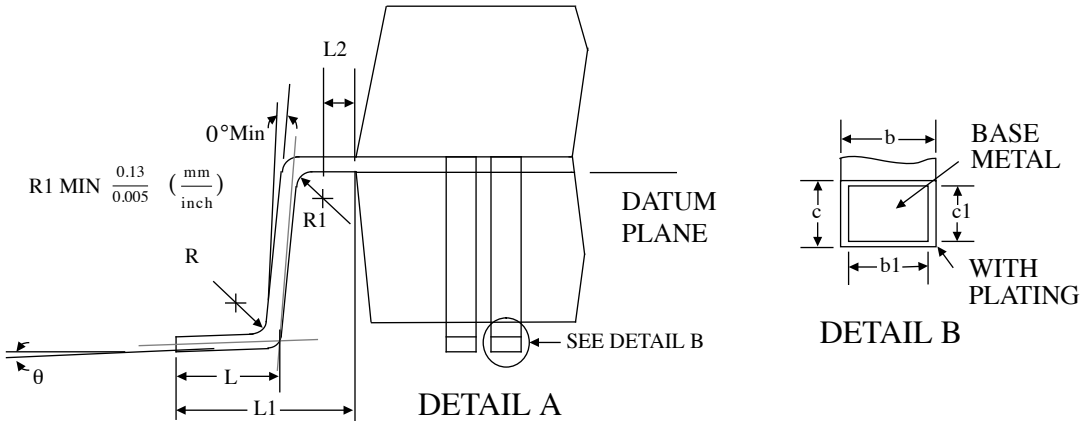


Figure 2-30 Mechanical Packaging Specification (Detail A and B)

Table 2-20 Package Measurements (mm)

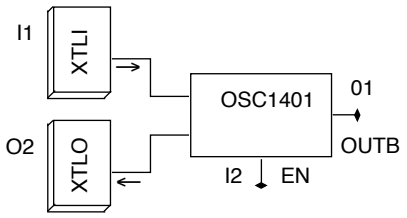
SYM	MIN.	NOM.	MAX.
A	—	—	4.07
A1	0.25	—	—
A2	3.17	3.42	3.67
D	31.65	31.90	32.15
D1	27.90	28.00	28.10
D3		25.35 Ref.	
E	31.65	31.90	32.15
E1	27.90	28.00	28.10
E3		25.35 Ref.	
L	0.65	0.80	0.95
L1		1.95 Ref.	
L2	0.40	—	—
e		0.65 BSC.	
b	0.22	—	0.38
b1	0.22	0.30	0.33
c	0.13	—	0.23
c1	0.13	—	0.17
R	0.13	—	0.40
θ	0°	—	7°

OSC1401 Crystal Oscillator

Features

- 20–50 MHz operation
- Buffered on-chip output
- Power-down mode
- gm = 72 mA/V typical

Inputs: XTLI, EN
Outputs: OUTB, XTLO
Kit Part: OSCHIP 1-A



Description

OSC1401 is a Pierce-type highfrequency crystal oscillator cell designed to operate from 25 MHz to 50 MHz. It is also possble to operate the OSC1401 as a crystal oscillator down to 3 MHz. Lower frequency operation may be desired if the frequency range of the IC product extends below 25 MHz as well as between 25 and 50 MHz.

Designs using a fundamental mode crystal require two external tuning capacitors and a resistor to complete the oscillator circuit. The resistor, R1, shown in Figure 2-10will be required to provide adequate phase shift at the lower fundamental frequencies. Typical values for R1 will be 100 ohms at 25 MHz to several hundred ohms at 10 MHz.

Fundamental mode crystals are not as easy to obtain above 25 or 30 MHz so oscillators in this frequency range are often designed to use a third overtone crystal. An additional inductor and coupling capacitor are required for overtone operation. Overtone operation from 25 to 50 MHz may also require a resistor in series with C_2 to optimize performance (see the overtone circuit shown in Figure 2-11.

A power-down mode allows the oscillator to be turned off when it is not needed, to conserve power. This is especially useful in battery powered applications. The EN (ENable) pin must be high for normal operation and lowfor power-down mode. In power-down mode the self-bias device, MP1, is turned off and the XTLI input is pulled to ground by an open drain n-channel FET. This causes XTLOand OUTB to go to a logic 1. Note that the buffer between XTLOand OUTB is noninverting.

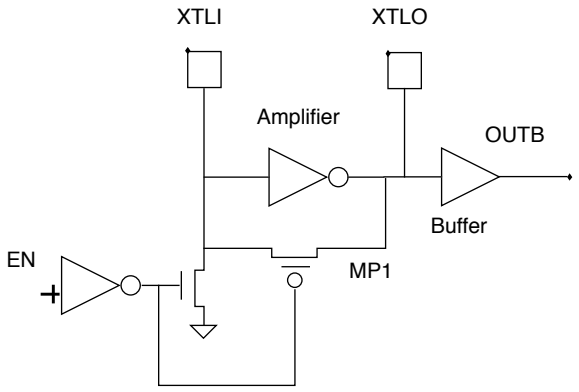


Figure 2-31 Functional Diagram

When EN is changed from low to high the oscillator may require several milliseconds to start-up and produce a stable output. The start-up time is dependent upon crystal parameters, especially the motional inductance of the crystal, L, as shown in Figure 2-12. A higher inductance value causes a slower start-up time. The analysis of startup time is beyond the scope of this data sheet but is covered in the references.

Preferred locations for OSC1401 are near the center of any side of the packaged part to minimize bond wire and lead frame parasitics. This is especially important in DIP packages. It is also desirable to place power (V_{DD}) and ground (V_{SS}) pins near the oscillator cell. A short, wide circuit board ground trace must be used from the V_{SS} pin(s) to the external tuning capacitors, C_1 and C_2. It is also important to provide a 0.01 µF or 0.1 µF bypass capacitor from V_{DD} to V_{SS} (very close to the pins) for proper oscillator operation.

Driving External Circuits

To drive external circuits with an oscillator generated clock, the on-chip oscillator output (OUTB) should drive a pad buffer such as OUTINV, which in turn drives an output pad such as an OPD8. A special output pad cell, the OPD16SYM, may be driven directly by the oscillator OUTB port without a buffer. This method provides the best possible waveform symmetry for driving external CMOS level circuits since the OPD16SYM has symmetrical low-high and high-low output drive. The oscillator output, XTLO, should not normally be used to drive external circuits except the oscillator components. To avoid undesired parasitic feedback paths, separate power and ground pins must be used to isolate the oscillator cell when it drives any pad cell, with or without an intermediate buffer.

Driving the OSC1401

In some cases, the user may want the option of driving the OSC1401 input with an external clock source rather than operating the cell as an oscillator. This may be the case if a clock source is available on the PC board of some products and not on others. The XTLI input can be driven with an external source provided XTLO is left unconnected. The maximum toggle frequency is typically 50 MHz with no load on XTLO. The signal driving XTLI must be from a CMOS driver such as standard 54/74HCxxx IC's or some other rail-to-rail driver. A TTL driver does not provide an adequate HI output level to drive the OSC1401 at high frequencies. Any application of the oscillator cell in which the input is driven should be first reviewed with an NCR applications engineer.

Theory and External Components

The internal bias device, MP1, causes the inverter to self bias to approximately $V_{DD}/2$. This is an operating point where the inverting amplifier has high gain, which is necessary for the circuit to oscillate. The on-resistance of MP1 is approximately 5 MΩ such that it will not affect the AC performance of the circuit.

Figures 2-11 and 2-12 show the external components required for fundamental and overtone operation. In Figure external components C_1, C_2 and the crystal, form a pi network which resonates at the specified crystal frequency. The ratio C_2/C_1 should be somewhat greater than unity since it is a term in the loop gain equation. Increasing the ratio too much will cause the voltage swing on XTLI to exceed the supply rails which is undesirable. Typically, a range of $1.1 < (C_2/C_1) < 1.5$ should be used.

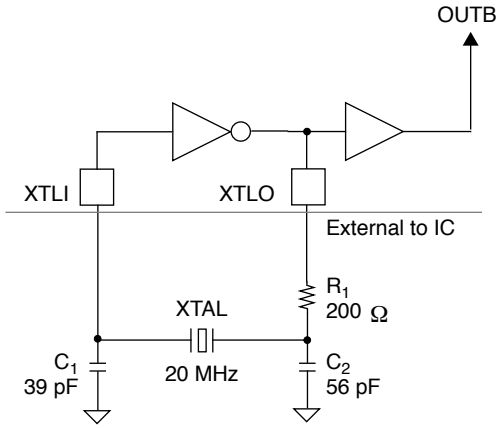


Figure 2-32 Typical Fundamental Mode Circuit

The series combination of C_2 and C_1 should also be approximately equal to the load capacitance specified for the quartz crystal. The strays associated with eachnode, and the oscillator input and output capacitance should be included in calculations which involve C_2 and C_1. Typical component values are shown in Figures 2-12 and 2-13.

The output resistance of the oscillator core, along with C_2, forms an RC low pass circuit. This pole contributes additional phase shift to insure that the phase shift around the loop is greater than 360 degrees, which is required for oscillation. In some cases the addition of a resistor in series with the output will improve performance and reduce the power supply current.

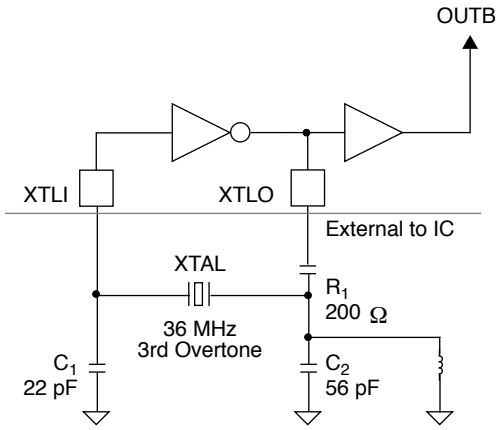


Figure 2-33 Typical Third Overtone Circuit

To achieve overtone oscillation, the crystal's fundamental mode must be suppressed by making the loop gain lower at the fundamental frequency compared to the third overtone frequency. An overtone crystal will resonate at its fundamental frequency unless the loop gain is forced to be higher at the overtone frequency. Loop gain must be less than one at the fundamental and greater than one at the desired overtone to insure startup on the overtone frequency.

Referring to Figure 2-11, the additional components necessary for overtone operation are a coupling capacitor and an inductor. The coupling capacitor is a DC block so the inductor does not short the inverter output to ground. In some cases a resistor in the range of 10-100 ohms in series with C_3 will improve the duty cycle and minimize supply current. C_3 is chosen such that its impedance is low compared to other components at the operating frequency. Values between 0.0015 μF and 0.01 μF are a good choice.

The inductor, L_1, is selected such that its impedance lowers the loop gain at the fundamental frequency relative to the third harmonic. The resonant frequency of the circuit made up of C_2 and L_1 is set midway between the fundamental and third overtone frequency. This causes the equivalent impedance to look inductive at the fundamental and capacitive at the third overtone frequency. The equivalent capacitance of C_2 and L_1 in parallel at the third overtone is used to calculate C_2 (effective) at the output node.

The value of C_1 may be reduced to as low as 10 pF since the input referred Miller capacitance actually increases the effective input capacitance beyond the specified values. Some experimentation with component values should be anticipated prior to specifying final production values. Refer to Table 2-23 for typical external component values.

Table 2-21 Typical Overtone Component Values

Third Overtone Frequency	C_1	C_2	L_1
25 MHz	33 pF	120 pF	0.68 μ
35 MHz	22 pF	100 pF	0.47 μH
50 MHz	22 pF	100 pF	0.22 μH
Note: C1 = 0.01 μF			

Crystals

The OSC1401 is a Pierce type oscillator circuit in which the crystal is operated in its parallel resonant mode. (Refer to the crystal equivalent circuit - Figure 2-12.) At parallel resonance, the LRC leg appears slightly inductive and resonates with C_0 and the circuit load capacitances, C_1 and C_2. Typical equivalent circuit component values are shown in Table 2-20. The values should only be used as a guideline in selecting a crystal for your application. The R_{MAX} column, however, should be adhered to when specifying a crystal. It will ensure a quality crystal which will resonate in a circuit using the OSC1401 cell.

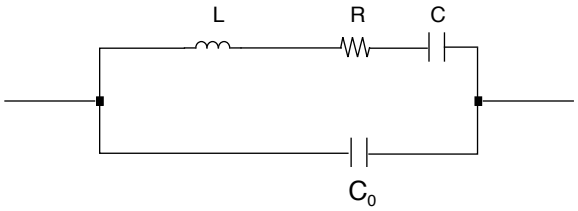


Figure 2-34 Crystal Equivalent Circuit

Simulation and Test

For simulation purposes, the XTLI to XTLO propagation delay is zero. In production test, the XTLO pin will be driven with the complement of the XTLI test signal. This is transparent to the designer.

The most thorough method of testing an oscillator circuit is to determine phase margin and gain by breaking the loop and making measurements with a network analyzer. A very basic test is observing the output waveform at XTLO on an oscilloscope when Vdd is first turned on, and in steady state. A FET probe should be used to keep capacitive loading to less than 2 pF. A standard 10X probe has an input capacitance of approximately 13 pF which will change the characteristics of the oscillator loop. A buffered output, which is available on the kit part, should be monitored if a standard probe is to be used.

Table 2-22 Typical Measured Crystal Parameters (Represents Several Manufacturers' AT Cut Crystals)

Crystal Frequency	L	C	C0	R	R_{MAX}
10 MHz	10.64 mH	23.83 fF	5.998 pF	14 Ω	30 Ω
20 MHz	3.042 mH	20.81 fF	5.310 pF	6.7 Ω	25Ω
24 MHz	25.005 mH	1.762 fF	4.095 pF	19 Ω	50Ω
36 MHz	13.321 mH	1.467 fF	6.88 pF	32 Ω	50Ω
48 MHz	6/997 mH	1.571 fF	6.407 pF	23 Ω	50Ω

Specifications

Table 2-23 Electrical Specifications

Parameter	Min	Typical @ 25 °C	Max	Unit	Operating Temp. Range °C	Comments/ Conditions
Power supply range	4.5		5.5	V	-55 to 125	
Amplifier transconductance (gm)	49 47 38 38	72	106 120 120 125	mmhos (mA/V)	25 0 to 70 -40 to 85 -40 to 125 -55 to 125	V_{DD} = 5.0 ± 10% Note 4

Note 1 - Some experimentation with external component values should be anticipated prior to specifying production values to achieve the duty cycle specifications shown.
Note 2 - DC bias voltage of core inverter input and output (XTLI and XTLO) with no crystal in the circuit.
Note 3 - Start-up time is dependent on the external circuit and the specific crystal being used. Start-up time is defined as the time required for the envelope of the XTLO output to reach 90% of final amplitude. This insures that OUTB is a valid clock.
Note 4 - At operating temperatures above 85 °C the load capacitance (CL) must be reduced below 32 pF for adequate gm margin at higher frequencies.

Table 2-23 Electrical Specifications (Continued)

Parameter	Min	Typical @ 25 °C	Max	Unit	Operating Temp. Range °C	Comments/ Conditions
Input capacitance (CXTLI)	8.3 8.3 8.3 8.3	11.9	16.0 16.0 16.0 16.0	pF	25 0 to 70 -40 to 85 -40 to 125 -55 to 125	V_{DD} = 5.0 ± 10%
Output capacitance (CXTLO)	4.5 4.5 4.5 4.5	6.1	8.1 8.1 8.1 8.1	pF	25 0 to 70 -40 to 85 -40 to 125 -55 to 125	V_{DD} = 5.0 ± 10%
Duty cycle	45 45 45 45	50	55 55 56 57	%	25 0 to 70 -40 to 85 -40 to 125 -55 to 125	At OUTB output Note 1
Self bias voltage		2.50		V	25	V_{DD} = 5.0 V Note 2
Startup time		2.0		mS	25	Note 3
Power-down (EN=0) supply current				µA		

Note 1 - Some experimentation with external component values should be anticipated prior to specifying production values to achieve the duty cycle specifications shown.

Note 2 - DC bias voltage of core inverter input and output (XTLI and XTLO) with no crystal in the circuit.

Note 3 - Start-up time is dependent on the external circuit and the specific crystal being used. Start-up time is defined as the time required for the envelope of the XTLO output to reach 90% of final amplitude. This insures that OUTB is a valid clock.

Note 4 - At operating temperatures above 85 °C the load capacitance (CL) must be reduced below 32 pF for adequate gm margin at higher frequencies.

Table 2-24 Power Supply Current – Overtone Mode

Supply Current	Operating Temp. °C
I_{DD} = 11.0 mA + (0.1 mA/MHz) x f (typical)	25
I_{DD} = 19.0 mA + (0.1 mA/MHz) x f (maximum)	0 to 70
I_{DD} = 20.0 mA + (0.1 mA/MHz) x f (maximum)	-40 to 85
I_{DD} = 20.0 mA + (0.1 mA/MHz) x f (maximum)	-40 to 125
I_{DD} = 20.5 mA + (0.1 mA/MHz) x f (maximum)	-55 to 125
Note: f = frequency in MHz (between 25 - 50 MHz)	

Table 2-25 Power Supply Current – Fundamental Mode

Supply Current	Operating Temp. °C
I_{DD} = 6.0 mA + (0.2 mA/MHz) x f (typical)	25
I_{DD} = 11.0 mA + (0.2 mA/MHz) x f (maximum)	0 to 70
I_{DD} = 12.0 mA + (0.2 mA/MHz) x f (maximum)	-40 to 85
I_{DD} = 12.0 mA + (0.2 mA/MHz) x f (maximum)	-40 to 125
I_{DD} = 12.5 mA + (0.2 mA/MHz) x f (maximum)	-55 to 125
Note: f = frequency in MHz (between 25 - 35 MHz) with a fundamental mode crystal.	