Bipolar Integrated Technology, Inc.

Preliminary

B5210

BIT SPARC Register File

FEATURES

- 8 ns worst case clocked read/write cycle time
- True multiport architecture, all ports can be active concurrently
- Five independently addressable ports:
  - Two read ports
  - Two write ports
  - One read/write bidirectional port
- Choice of latch or edge-triggered registers for read addresses and data
- Transparent latches permit flowthrough read operations
- Separate read and write clocks permit asynchronous operations
- Write-through in one cycle
- Individual write and output enables for easy cascading
- Provision for double precision operations from adjacent addresses
- Self-timed write pulse eases clock skew problems
- 168-lead pin grid array package
- ECL 10KH compatible
- 7 watts nominal power dissipation

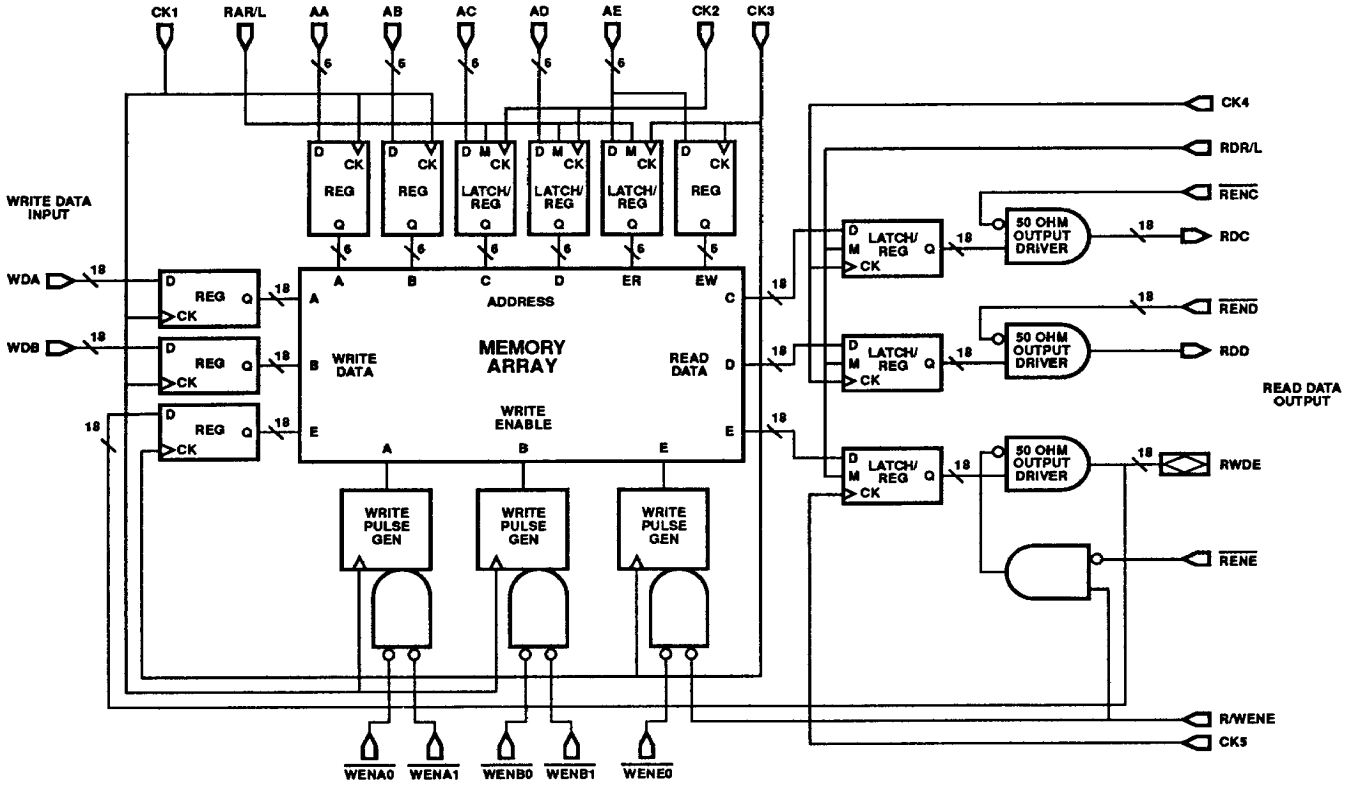
DESCRIPTION

The B5210 is a high speed 1152-bit register file fabricated with BIT's high speed bipolar technology. The device is organized as 64, 18-bit words, and is intended for use with the B5100 BIT SPARC Floating Point Controller. This five port register file has been designed to allow Bipolar Integrated Technology's high speed data path elements to operate at maximum rates.

Five independently addressable ports, with separate read and write clocks permit asynchronous, concurrent access to the memory array. The B5210 has two read ports, two write ports, and one bidirectional read/write port. System design flexibility is enhanced with the choice of transparent latches or edge-triggered registers for read addresses and data. Data can be written to and read from the same word in the same cycle to allow the result of an operation to be fed back to the inputs for additional processing. Individual write and output enables on each port allow multiple register files to be cascaded to form deeper memory buffers. An additional least significant address pin is "ored" with the least significant bit of the read, write, and read/write ports to support double-word operand accesses. This feature is useful in transferring double precision operands when the most significant and least significant words are at contiguous memory locations.

A write enable pulse is internally generated after data and address updates are clocked into the write input registers. This feature reduces address and data setup and hold time requirements.

BLOCK DIAGRAM



SIGNAL SUMMARY

Data		
Write Ports A,B	WDA[17..0], WDB[17..0]	36
Read Ports C,D	RDC[17..0], RDD[17..0]	36
Read/Write Port E	R/WDE[17..0]	18
Address		
Ports A,B,C,D,E	AA[5..0], AB[5..0], AC[5..0], AD[5..0], AE[5..0]	30
Odd/Even R,W R/W	AWO, ARO, AR/WO	3
Control		
Register/Latch	RARM, RDFM	2
Write Enables	WENA[1..0], WENB[1..0], WENE0	5
Read Output Enables	RENC, REND, RENE	3
Read/Write Enable	R/WENE	1
Clocks		
Ports A,B Write	CK1	1
Ports C,D Read Address	CK2	1
Port E Write, E Read Address	CK3	1
Ports C,D Read Data	CK4	1
Port E Read Data	CK5	1
Power		
Logic Gnd	VCC1	14
Output Gnd	VCC2	8
-5.2 V	VEE	7
Total		168

SIGNAL DESCRIPTION

Data

WDA[17..0]	Input data lines for write port A.
WDB[17..0]	Input data lines for write port B.
RDC[17..0]	Output data lines for read port C.
RDD[17..0]	Ouput data lines for read port D.
R/WDE[17..0]	Bidirectional data lines for read/write port E.

Address

AA[5..0]	Address lines for write port A.
AB[5..0]	Address lines for write port B.
AC[5..0]	Address lines for read port C.
AD[5..0]	Address lines for read port D.
AE[5..0]	Address lines for read/write port E.
AWO	Additional pin logically 'ored' to the LSB's of the write addresses on write only ports (A and B).
ARO	Additional pin logically 'ored' to the LSB's of the read addresses on read only ports (C and D).
AR/WO	Additional pin logically 'ored' to the LSB of the read/write address for the bi-directional port (E).

Clocks

CK1	Clock for write ports A and B. Addresses and data are entered into the registers and the write pulse is generated on the rising edge of the clock.
CK2	Clock/enable for ports C and D. Read addresses are entered into the registers on the rising edge of the clock. When configured as a latch the read address enable is active low.
CK3	Clock/enable for read/write port E. The write address and write data are entered into the registers and the write pulse is generated on the rising edge of the clock. The read address is entered into the register on the rising edge of the clock. When configured as a latch the read address enable is active low.
CK4	Clock/enable for ports C and D read data registers/latches. Read data is entered into the register on the rising edge of the clock. When configured as a latch the read data enable is active high.
CK5	Clock/enable for port E's read data registers/latches. Read data is entered into the registers on the rising edge of the clock. When configured as a latch the read data enable is active high.

Control

RAR/L — Read address register/latch mode control. The read address registers are configured as transparent latches when RAR/L is low. The read address registers are configured as rising edge triggered flip-flops when RAR/L is high.

RDR/L — Read data register/latch mode control. The read data registers are configured as transparent latches when RDR/L is low. The read data registers are configured as rising edge triggered flip-flops when RDR/L is high.

$\overline{\text{WENA0}}$ — Write enable for port A. A write pulse is generated for port A only when WENA0 and $\overline{\text{WENA1}}$ are both low during the rising edge of CK1.

$\overline{\text{WENA1}}$ — Write enable for port A. A write pulse is generated for port A only when WENA0 and $\overline{\text{WENA1}}$ are both low during the rising edge of CK1.

$\overline{\text{WENB0}}$ — Write enable for port B. A write pulse is generated for port B only when WENB0 and $\overline{\text{WENB1}}$ are both low during the rising edge of CK1.

$\overline{\text{WENB1}}$ — Write enable for port B. A write pulse is generated for port B only when WENB0 and $\overline{\text{WENB1}}$ are both low during the rising edge of CK1.

$\overline{\text{WENE0}}$ — Write enable for port E. A write pulse is generated for port E only when $\overline{\text{WENE0}}$ and R/$\overline{\text{WENE}}$ are both low during the rising edge of CK3

R/$\overline{\text{WENE}}$ — Read/write control for port E. A write pulse is generated for port E only when $\overline{\text{WENE0}}$ and R/$\overline{\text{WENE}}$ are both low during the rising edge of CK3. The outputs of port E are all low when R/$\overline{\text{WENE}}$ is low.

$\overline{\text{RENC}}$ — Output enable for port C. The outputs ofport C are all low when $\overline{\text{RENC}}$ is high.

$\overline{\text{REND}}$ — Output enable for port D. The outputs of port D are all low when $\overline{\text{REND}}$ is high

$\overline{\text{RENE}}$ — Output enable for port E. The outputs of port E are all low when $\overline{\text{RENE}}$ is high.

Power

VCC1 — Most positive power supply voltage to the internal circuitry. Usually ground.

VCC2 — Most positive power supply voltage to the output circuitry. Usually ground.

VEE — Most negative supply voltage.

■ FUNCTIONAL DESCRIPTION

Read Cycle

The B5210 provides user configurable latches (RAR/L = RDR/L = 0) or edge triggered registers (RAR/L = RDR/L = 1) on address inputs and data outputs for each read port. CK2 clocks addresses into the input registers/latches for read ports C and D, while CK4 clocks data into the output registers/latches for ports C and D. CK3 clocks read addresses into the input register/latch for the bidirectional E port, while CK5 clocks data into the output register/latch for port E.

When RAR/L and RDR/L are low, the register file is in latch mode and the address and data latches can be used as a master/slave pair. In this case, the read address and data clocks will typically be tied together externally.

Write Cycle

The B5210 provides rising edge triggered registers on data and address ports. CK1 clocks addresses and data into the input register for write ports A and B. Write addresses and data are clocked into port E with CK3.

A write cycle will be initiated only if $\overline{\text{WENX[1..0]}}$ is low. WENX[1..0] is internally latched on the rising edge of the write clock (CK1, CK3). The cycle will be completed on the falling edge of the write clock. Write through cycles are possible in which new data is written to and read from the same address at the same time. This allows the result of a computation to be "written through" the register file to the input read data register/latch. The read cycle is extended during these cycles. See the read cycle timing diagrams for additional information.

Concurrent write operations to the same address produce indeterminate results. However, concurrent write operations to different addresses will produce correct results.

Output Enables

The read port data lines are designed to drive 50Ω transmission lines terminated to -2 volts. When disabled by $\overline{\text{RENC}}$, $\overline{\text{REND}}$, $\overline{\text{RENE}}$ or R/$\overline{\text{WENE}}$, the outputs are low.

Absolute Maximum Ratings

Permanent damage may occur if any one absolute maximum rating is exceeded. Functional operation is not implied and device reliability may be impaired by exposure to higher than Recommended Operating and Test Conditions for extended periods of time.

Parameter	Symbol	Value		Units
		With Heatsink	Without Heatsink	
Supply Voltage	V_{ee}	-7.0 to 0	-7.0 to 0	V_{dc}
Input Voltage	V_{in}	V_{ee} to 0	V_{ee} to 0	V_{dc}
Output Source Current				
Continuous	I_{oc}	30	30	mA_{dc}
Surge	I_{os}	100	100	mA_{dc}
Max Storage Temperature	T_{st}	125	150	°C
Max Junction Temperature	T_j	125	225	°C

Recommended Operating and Test Conditions

The following environmental conditions pertain to guaranteed DC and Switching characteristics. These conditions should not be exceded during normal operation.

Parameter	Symbol	Min	Nom	Max	Units
Supply Voltage	V_{ee}	-5.46	-5.20	-4.94	V_{dc}
Junction Temperature	T_{jo}[1]	15		111	°C
Output Termination to -2.0V_{dc}	R_t		50		Ω

Note 1: Worst case junction temperature specified for worst case I_{ee}.

DC Characteristics

Parameter	Symbol	Min	Nom	Max	Units
Supply Current	I_{ee}	-0.9		-1.7	A_{dc}
Input Current High	I_{ih}			0.3	mA_{dc}
Input Capacitance	C_{in}		5		pF

Parameter	Symbol	T_{jo} Min		T_{jo} Nom		T_{jo} Max		Units
		Min	Max	Min	Max	Min	Max	
Input Voltage High	V_{ih}	-1.17		-1.13		-1.07		V_{dc}
Input Voltage Low	V_{il}		-1.48		-1.48		-1.45	V_{dc}
Output Voltage High	V_{oh}	-1.02		-0.98		-0.92		V_{dc}
Output Voltage Low	V_{ol}		-1.63		-1.63		-1.60	V_{dc}

Switching Characteristics

Parameter	Symbol	Min	Max	Units
Setup Time				
Ports A, B	t_{ws}	1.0		ns
Ports C, D	t_{rs}	2.0		ns
Port E (Write data)	t_{rws}	2.0		ns
Port E (All else)	t_{rws}	2.5		ns
Hold Time				
Ports A, B	t_{wh}	2.0		ns
Ports C, D	t_{rh}	1.5		ns
Port E	t_{rwh}	1.8		ns
Pulse Duration High	t_{ch}	4.0		ns
Pulse Duration Low	t_{cl}	4.0		ns
Read Cycle - Register to Register				
Register to Register Hold Time	t_{rrh}	0.0		ns
Registered Address to Registered Data Time	t_{rra}		8.0	ns
Read Cycle - Register to Latch				
Latch to Register Hold Time	t_{lrh}	0.0		ns
Registered Address to Latched Data Time	t_{rla}		8.0	ns
Registered Address to Data Access Time	t_{rda}		10.0	ns
Read Cycle - Latch to Register				
Register to Latch Hold Time	t_{rlh}	0.0		ns
Latched Address to Registered Data Time	t_{lra}		8.0	ns
Address to Registered Data Time	t_{dra}		8.0	ns
Read Cycle - Latch to Latch				
Latch to Latch Hold Time	t_{llh}	0.0		ns
Latched Address to Latched Data Time	t_{lla}		8.0	ns
Address to Latched Data Time	t_{dla}		8.0	ns
Address to Data Access Time	t_{dda}		10.0	ns
Latched Address to Data Access Time	t_{lda}		10.0	ns

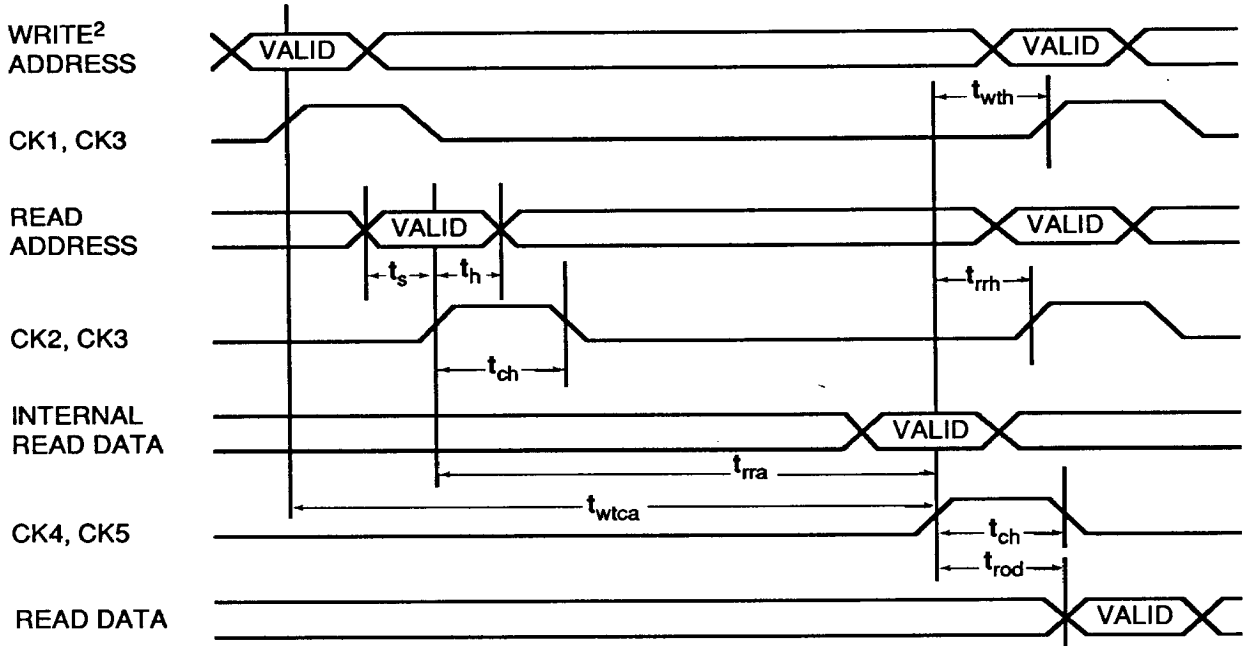
Switching Characteristics (Cont'd)

Parameter	Symbol	Min	Max	Units
Write Cycle				
Write Cycle Time	t_{wc}	8.0		ns
Output Timing				
Register Output Delay	t_{rod}	1.0	6.5	ns
Latch Output Delay	t_{lod}	1.0	6.5	ns
Output Disable Time	t_{dao}	0	6.5	ns
Output Enable Time	t_{eno}	0	6.5	ns
Write Through Cycle				
Clocked Write Through Time	t_{wtca}		10.0	ns
Write Through Access Time	t_{wta}		13.0	ns
Write Through Hold Time	t_{wth}	0.0		ns

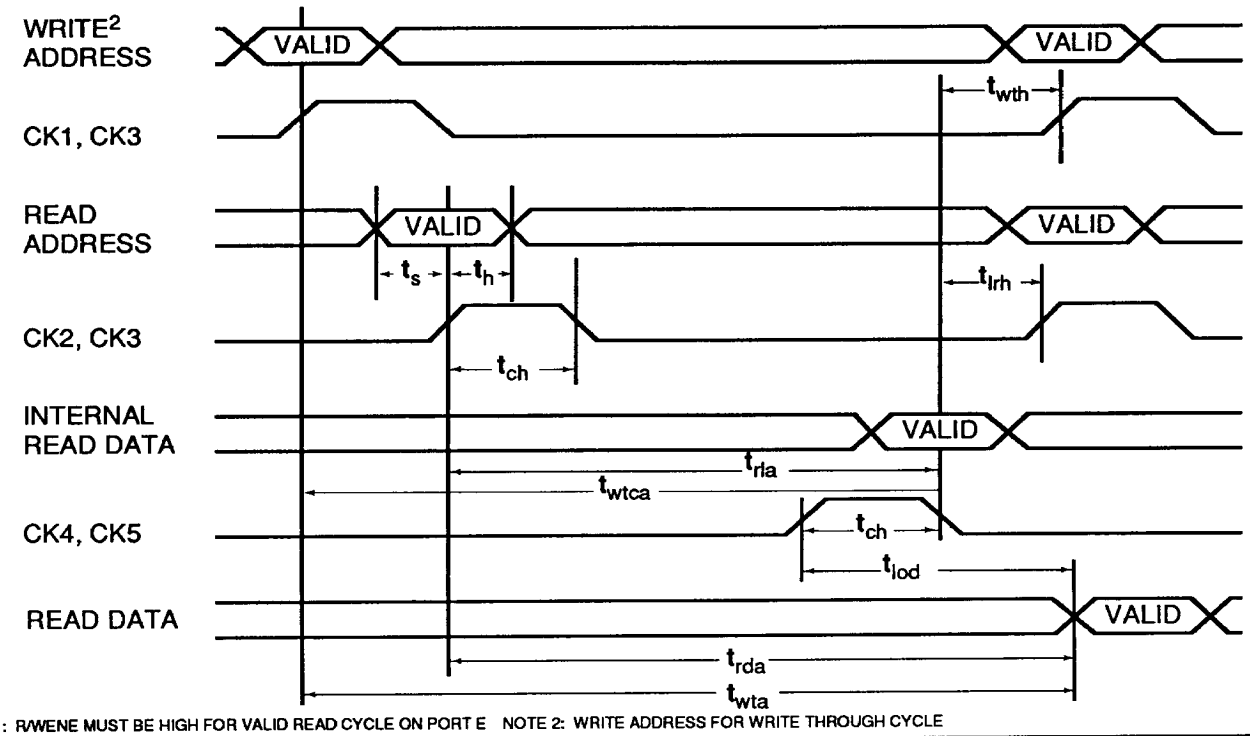
■ TIMING DIAGRAMS

READ CYCLE PORTS C, D, AND E[1]

REGISTER TO REGISTER (RAR/L = RDR/L = 1)



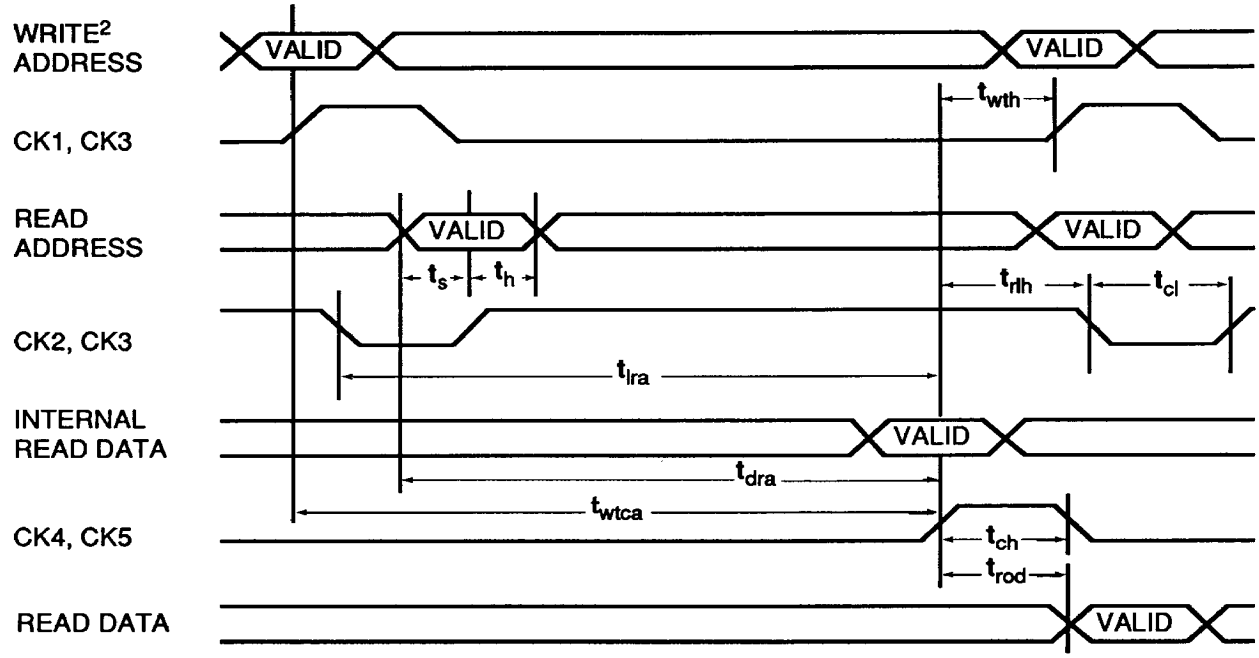
REGISTER TO LATCH (RAR/L = 1, RDR/L = 0)



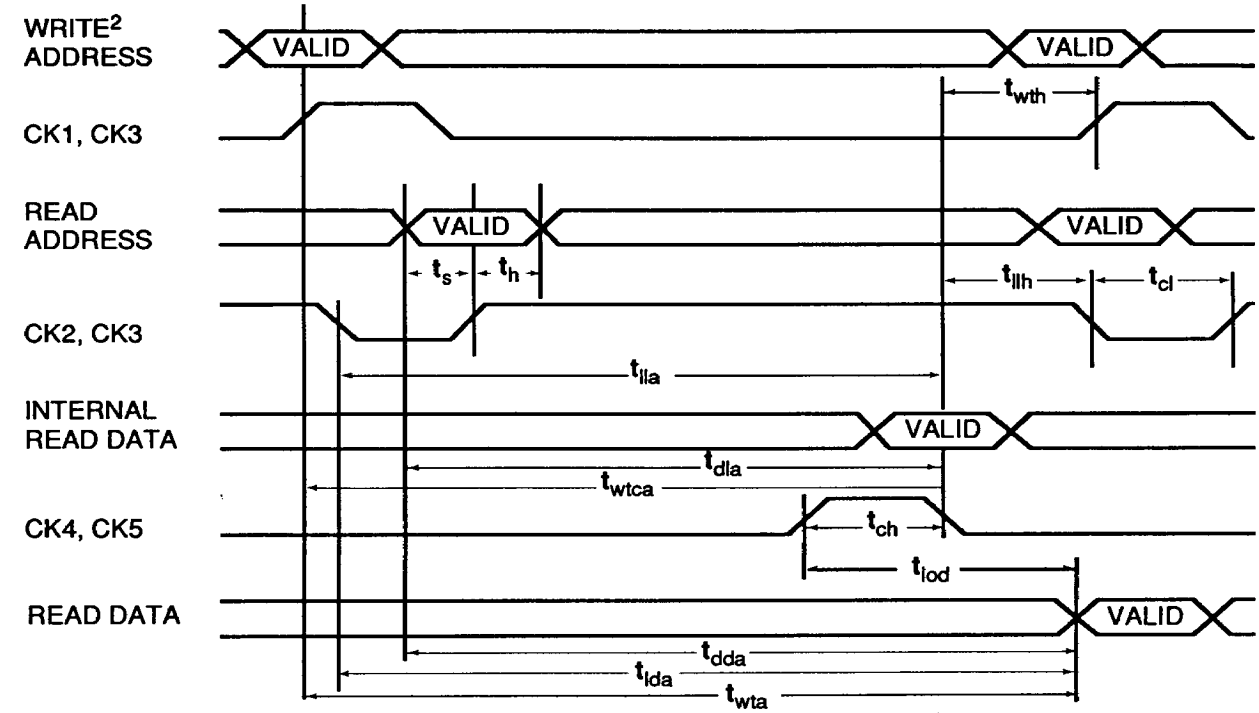
NOTE 1: R/WENE MUST BE HIGH FOR VALID READ CYCLE ON PORT E NOTE 2: WRITE ADDRESS FOR WRITE THROUGH CYCLE

READ CYCLE PORTS C, D, AND E[1]

LATCH TO REGISTER (RAR/L = 0, RDR/L = 1)

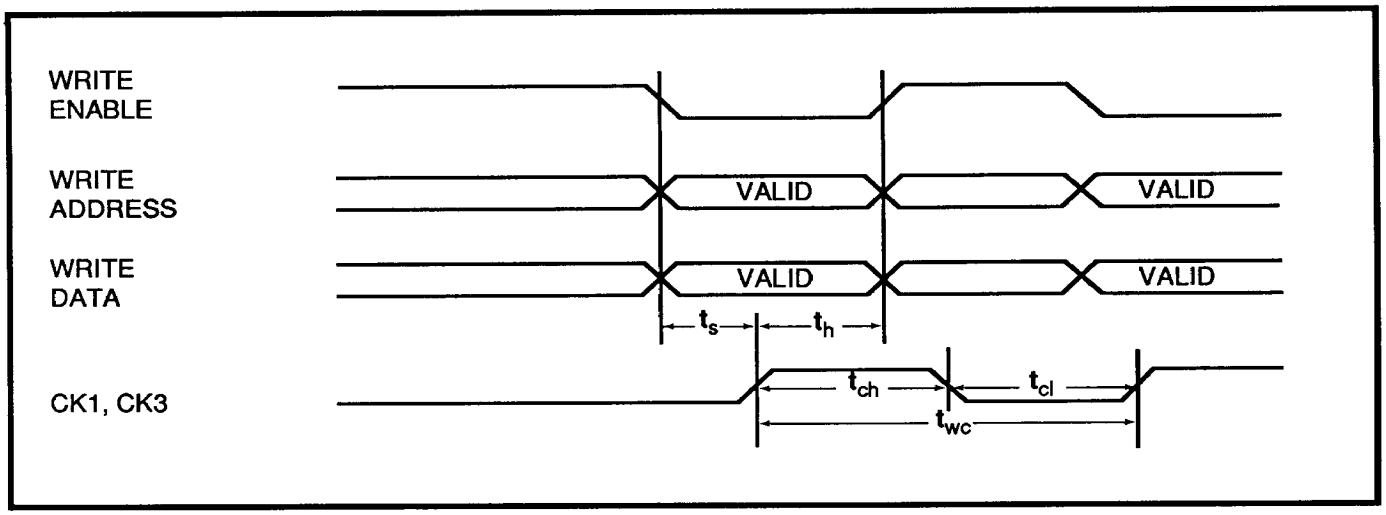


LATCH TO LATCH (RAR/L = RDR/L = 0)



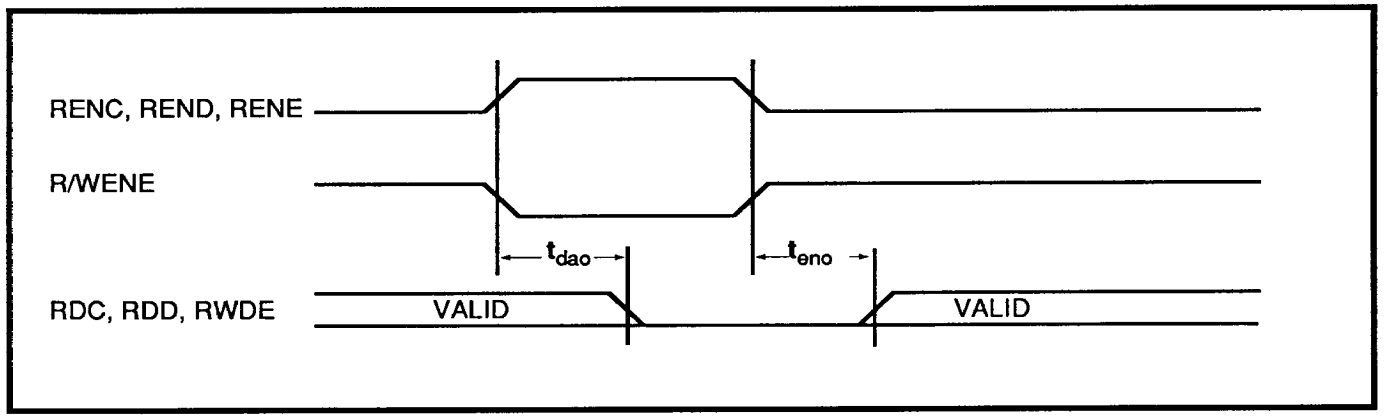
NOTE 1: R/WENE MUST BE HIGH FOR VALID READ CYCLE ON PORT E NOTE 2: WRITE ADDRESS FOR WRITE THROUGH CYCLE

WRITE CYCLE PORTS C, D, AND E[3]



NOTE 3: R/WENE MUST BE LOW FOR VALID WRITE CYCLE ON PORT E

OUTPUT ENABLE



NOTE: t_s may include t_{rs}, t_{ws}, and/or t_{rws}.
t_h may include t_{rh}, t_{wh} and/or t_{rwh}.

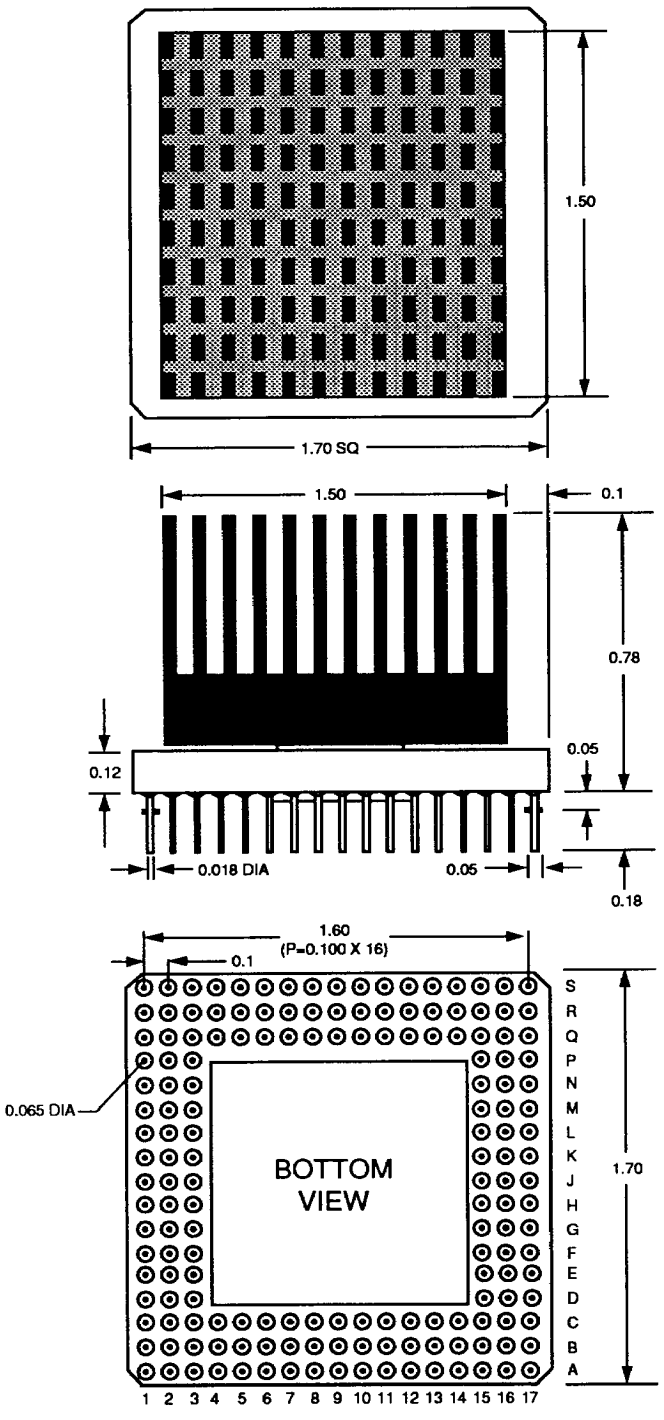
PIN OUT

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	
S	VCC1	VCC1	VCC2	VEE	VEE	RDC12	VCC1	VCC1	VCC2	RDD1	VCC1	VCC1	VCC2	VEE	VCC1	VEE	RDD17	S
R	RAR/L	RDC4	RDC5	RDC7	RDC9	RDC11	RDC14	RDC16	RDD0	RDD2	RDD5	RDD6	RDD8	RDD10	RDD12	RDD13	AWO	R
Q	VCC2	RDC0	RDC3	RDC6	RDC8	RDC10	RDC13	RDC15	RDC17	RDD3	RDD4	RDD7	RDD9	RDD11	RDD14	RDD16	VCC2	Q
P	CK1	RDC1	RDC2												RDD15	AR/W0	$\overline{\text{WENA1}}$	P
N	CK4	CK2	RDR/L												$\overline{\text{WENA0}}$	$\overline{\text{WENB0}}$	$\overline{\text{WENB1}}$	N
M	CK5	$\overline{\text{RENC}}$	AR0												$\overline{\text{WENE0}}$	RWENE	AE5	M
L	AD5	$\overline{\text{REND}}$	CK3												AE4	AE3	AE2	L
K	AD3	AD4	$\overline{\text{RENE}}$												AE1	AE0	AB5	K
J	AD0	AD2	AD1												AB2	AB3	AB4	J
H	AC5	AC4	AC3												AA5	AB0	AB1	H
G	AC2	AC1	AC0												AA2	AA3	AA4	G
F	WDB17	WDB16	WDB15												WDA16	AA0	AA1	F
E	WDB14	WDB13	WDB12												WDA14	WDA15	WDA17	E
D	WDB10	WDB11	WDB9												WDA10	WDA11	WDA13	D
C	WDB8	WDB7	WDB5	WDB2	R/WDE1	R/WDE3	R/WDE6	R/WDE9	R/WDE11	R/WDE13	R/WDE15	R/WDE17	WDA1	WDA3	WDA8	WDA12	WDA9	C
B	WDB6	WDB4	WDB3	WDB0	R/WDE0	R/WDE4	R/WDE7	R/WDE8	R/WDE10	R/WDE12	R/WDE14	R/WDE16	WDA0	WDA2	WDA6	WDA7	VCC1	B
A	VCC1	VCC1	WDB1	VCC2	VEE	R/WDE2	R/WDE5	VEE	VCC1	VCC1	VCC2	VEE	VCC1	VCC2	WDA4	WDA5	VCC1	A
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	

Five Port Register File
168 Pin PGA Pinout

B5210
BOTTOM
VIEW

■ PACKAGING DRAWING AND DIMENSIONS



A1 Identification Marked on Top

■ ORDERING INFORMATION

B5210 - X

Packaging Option/
Screening Option:

- Blank – Standard heatsink attached.
- S – No heatsink attached; refer to MKTG-T002 for thermal guidelines.
- B – Standard heatsink attached with Burn-in.
- E – No heatsink attached with Burn-in; refer to MKTG-T002 for thermal guidelines.

Device Number
B5210 – BIT SPARC Register File

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