

Dual 50 MHz SuperSPARC MBus Module™

DATA SHEET

Dual SuperSPARC + E-Cache Module

DESCRIPTION

The STP5022B is a dual SuperSPARC based MBus module. It is designed with the latest high performance superscalar SuperSPARC microprocessors (STP1020A) and the latest External Cache controllers that are known as the MXCCs (STP1090A). This module provides the benefit of two CPU subsystems with External Cache using a single MBus connector. Each SuperSPARC has 1MB of secondary cache. Using two of these modules, an SS10 or an SS20 can be configured as a 4-way multiprocessing system. This module is targeted for high performance desktops and servers. The SuperSPARC integrates integer and floating point execution units, memory management unit (MMU), and large level-1 instruction and data caches (total of 36 KBytes of cache memory). The STP1020A uses the VBus interface to integrate with the MXCC and the E-Cache memory. Along with the SuperSPARC CPUs, the MXCCs, and the synchronous SRAMS, the STP5022B module also consists of two separate discrete voltage regulators that maintain the supply voltage to the SuperSPARCs within the required tolerance.

Features

- High performance dual SuperSPARC CPU module with 50 MHz of SuperSPARC operating frequency, and a total of 2MB of E-Cache
- Implements 40 MHz MBus
- Cache coherency support for multi-processing
- On-board voltage regulator module
- MBus compliant module design
- Fully tested CPU module
- MBus is implemented on 100-pin AMP / Fujitsu Microstrip connector

Benefits

- Delivers 73 SpecInt92, 85 SpecFp92, and 136 Dhrystone MIPS per CPU
- Functions in both SS20 (40 MHz MBus) and SS10 (40 MHz MBus)
- Allows a wide range of scalable systems to be built
- Eliminates complicated external voltage regulator design
- Removes Customer's CPU subsystem Design Cycle burden
- Reduces customers Testing Operations, allows faster Time to Market
- High performance impedance controlled connector

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TYPICAL STP5022B APPLICATIONS

The STP5022B is intended for use in a broad range of applications from desktop machines to large multiprocessor servers. A variety of high performance embedded applications can also be built around STP5022B modules and take advantage of their flexibility, scalability, and ease of design. A block diagram of a system with STP5022B interfacing directly with the rest of the system is shown below.

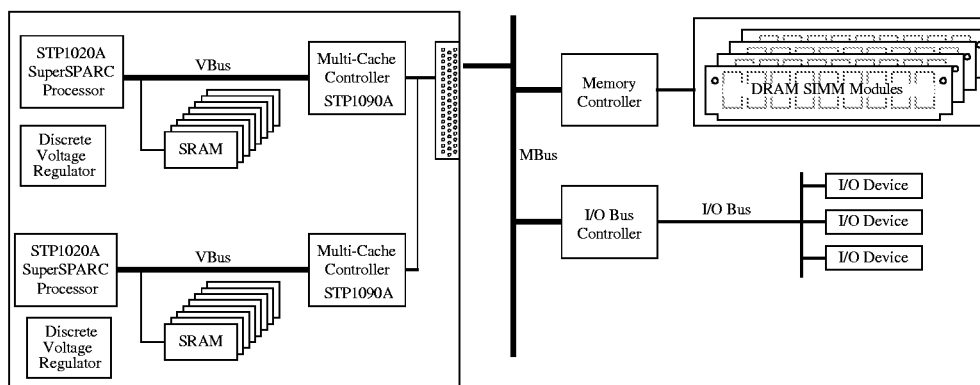


Figure 1. Typical STP5022B Based System

MBUS DESCRIPTION

MBus is a SPARC International standard bus designed to function as a processor-independent bus between one or more processors and memory. It is a 64-bit multiplexed high-performance bus. It is fully synchronous with all the transfers controlled by an MBus clock. It supports block transfers in sizes up to 128. All transactions on the MBus are arbitrated by an external arbiter. The arbitration algorithm is not included in the MBus definition to allow flexibility in system design. MBus is defined for uniprocessor and multiprocessor systems. The uniprocessor form of MBus is termed "Level1", and the multiprocessor version is called "Level2". The STP5022B can operate in either Level1 or Level2.

PCB BOARD

The PCB construction is designed to minimize impedance mismatches between boards in a system. The specification is 50 ohm $\pm 10\%$ impedance on all signal layers, and the signal propagation speed is 180 ps/inch with a tolerance of 20 ps/inch. The MCLK0, and MCLK2 signals are the clock inputs to the two MXCCs, and each one has a trace length of 12.8 inches. This is the length between the MBus connector and the MXCC MCLK pins. Adhering to the MBus specification, this trace is intentionally laid out to provide a minimum offset of 2ns (maximum offset of 2.6ns) between the MBus connector and the STP1090A MCLK pins.

MBUS CONNECTOR

The MBus connector is a high performance impedance controlled (50 ohm $\pm 10\%$) connector. The connector has 100 signal pins and 20 additional pins (5 blades) for power and ground. The MBus connector has high reliability and can be installed easily. It has excellent electrical performance, i.e., transmission line characteristics with low capacitance and inductance. The connector also has two separate power and three separate ground blades with 1 nH inductance. The suppliers of this connector are Fujitsu (part number: FCN-264P100-G/C) and AMP (part number: 121497-4). Mating connector to be used on the system board is also available Fujitsu and AMP (part number: 121340-4).

Following is the MBus signal pin definitions for the connector.

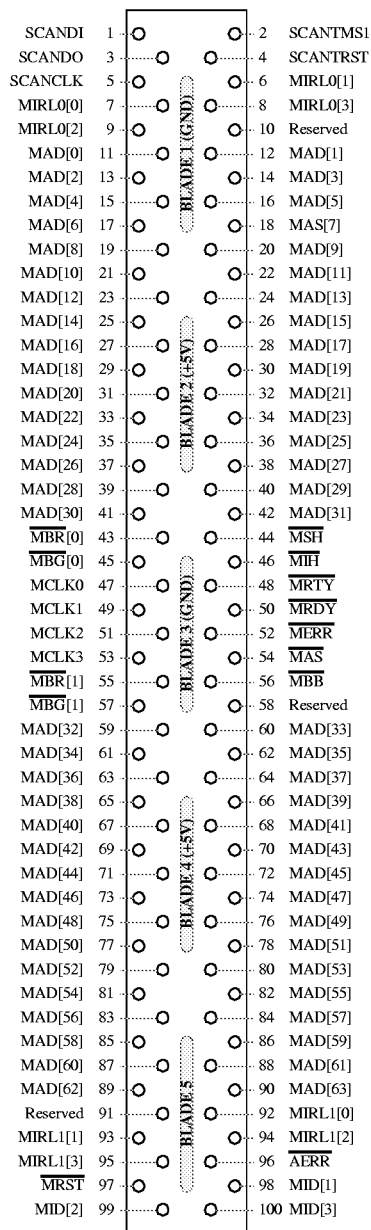


Figure 2. MBus Connector Pinout

STP5022B MODULE SIGNAL DESCRIPTIONS

Signal	Type	Description																																				
$\overline{\text{AERR}}^{[1]}$	O	In error mode, the STP5022B will perform an automatic watchdog reset. Error mode is entered when any exception is taken with traps disabled (PSR.ET=0). This signal is driven only when asserted; otherwise, it is in three-state. H = Normal operation. L = Error Mode.																																				
MCLK[3:0]	I	MBus clock generated on the on the motherboard.																																				
MAD[63:00]	I/O	Multiplexed Command / Data.																																				
$\overline{\text{MAS}}$	I/O	MBus address strobe. Asserted by the bus master when an MBus command word (containing address and control information) is on MAD63-MAD00. H = No command word. L = MBus command word on MAD63-MAD0.																																				
$\overline{\text{MBB}}$	I/O	MBus busy. Asserted when there is any active transaction on MBus. H = MBus free. L = MBus busy.																																				
$\overline{\text{MBG}}[0,1]$	I	MBus grant. This is a dedicated (not bussed) signal from the MBus arbiter to this bus master. H = Not granted. The STP5022B may not initiate an MBus transaction. L = Granted. The STP5022B may initiate an MBus transaction as soon as MBus is free.																																				
$\overline{\text{MBR}}[0,1]$	O	MBus request. This is a dedicated (not bussed) signal from the STP5022B to the MBus arbiter. H = No request. L = Requesting to initiate a transaction on MBus.																																				
$\overline{\text{MERR}}$	I	MBus error. Encoded along with $\overline{\text{MRDY}}$ and $\overline{\text{MRTY}}$ to indicate acknowledge type (the type of error response). <table><tr><th>$\overline{\text{MERR}}$</th><th>$\overline{\text{MRDY}}$</th><th>$\overline{\text{MRTY}}$</th><th>Description</th></tr><tr><td>H</td><td>H</td><td>H</td><td>Idle Cycle</td></tr><tr><td>H</td><td>H</td><td>L</td><td>Relinquish and Retry</td></tr><tr><td>H</td><td>L</td><td>H</td><td>Valid Data Transfer</td></tr><tr><td>H</td><td>L</td><td>L</td><td>Reserved</td></tr><tr><td>L</td><td>H</td><td>H</td><td>Bus Error (ERROR1)</td></tr><tr><td>L</td><td>H</td><td>L</td><td>Timeout Error (ERROR2)</td></tr><tr><td>L</td><td>L</td><td>H</td><td>Uncorrectable Error (ERROR3)</td></tr><tr><td>L</td><td>L</td><td>L</td><td>Retry</td></tr></table>	$\overline{\text{MERR}}$	$\overline{\text{MRDY}}$	$\overline{\text{MRTY}}$	Description	H	H	H	Idle Cycle	H	H	L	Relinquish and Retry	H	L	H	Valid Data Transfer	H	L	L	Reserved	L	H	H	Bus Error (ERROR1)	L	H	L	Timeout Error (ERROR2)	L	L	H	Uncorrectable Error (ERROR3)	L	L	L	Retry
$\overline{\text{MERR}}$	$\overline{\text{MRDY}}$	$\overline{\text{MRTY}}$	Description																																			
H	H	H	Idle Cycle																																			
H	H	L	Relinquish and Retry																																			
H	L	H	Valid Data Transfer																																			
H	L	L	Reserved																																			
L	H	H	Bus Error (ERROR1)																																			
L	H	L	Timeout Error (ERROR2)																																			
L	L	H	Uncorrectable Error (ERROR3)																																			
L	L	L	Retry																																			
MID[3:1]	I	MBus Module ID. The identifier of this MBus device. Usually hardwired by the system. MID3 is the Most Significant Bit (MSB).																																				
$\overline{\text{MIH}}$	I/O	Memory inhibit. Asserted by a snooping cache when it notices a coherent read of cache block it owns. Memory responds to this signal by ignoring the request. H = No memory inhibit. L = Inhibit memory. The snooping cache which asserted $\overline{\text{MIH}}$ will respond with the data in place of memory.																																				

STP5022B MODULE SIGNAL DESCRIPTIONS

Signal	Type	Description
MIRL0[3:0] MIRL1[3:0]	I	Interrupt request level. This field specifies the level of the highest priority interrupt request that is currently pending. If MIRL3-MIRL0 = 0000, no interrupts are pending. Level 15 (MIRL3-MIRL0 = 1111) is a NMI (disable all traps) Level 14 Highest maskable interrupt Level 1 Lowest maskable interrupt Level 0 No interrupts are pending
$\overline{\text{MRDY}}$	I/O	MBus ready. Encoded along with $\overline{\text{MERR}}$ and $\overline{\text{MRTY}}$ to indicate acknowledgment type (the type of error response). See table in $\overline{\text{MERR}}$ description.
$\overline{\text{MRTY}}$	I	MBus retry. Encoded along with $\overline{\text{MERR}}$ and $\overline{\text{MRDY}}$ to indicate acknowledgment type (the type of error response). See table in $\overline{\text{MERR}}$ description.
$\overline{\text{MSH}}^{[1]}$	I/O	Memory shared. Asserted by a snooping cache when it notices a coherent read of a cache block it is caching. Both caches will mark the data as shared. H = No sharing. L = Shared data.
$\overline{\text{MRST}}$	I	Reset In. This causes an external reset for the STP5022B. At power-on, $\overline{\text{RSTIN}}$ must be held low for at least 100 ms to all allow the PLL to stabilize. If the PLL is known to be stable, $\overline{\text{RSTIN}}$ may be asserted for as short as 8 cycles. Any time V_{CC} is not within specification both SCANTMS2 (pin 4) and $\overline{\text{MRST}}$ (pin 97) must be asserted to avoid internal and external driver fights. Both internal and external driver fights might damage the chips. H = Normal operation. L = The STP5022B is externally reset.
Reserved	NA	These pins are not used by the module. Leave these pins floating.
SCANCLK	I	JTAG test clock input.
SCANDI	I	JTAG test data input.
SCANDO	O	JTAG test data output.
SCANTMS1	I	JTAG test mode select input.
$\overline{\text{SCANTRST}}$	I	JTAG test reset input.

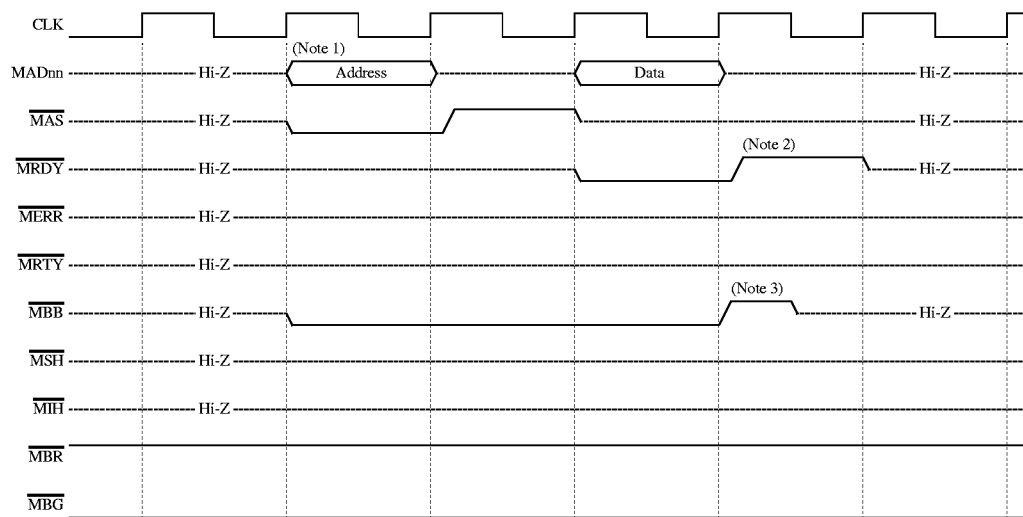
1. These pins have an open drain.

MBUS TIMING

The MBus read, write and invalidate operations are explained in the following section.

MBus Single Read

The single read cycle transfers a byte, half-word, word, or a double-word. Big-endian word ordering is used (the least significant bytes in a word appear on the high bits of the bus according to SPARC standard). *Figure 3* shows an MBus single read operation.



- Notes: 1. MADnn lines are held to their previously driven state by system bus holders.
 2. Control lines ($\overline{\text{MAS}}$, $\overline{\text{MRDY}}$, $\overline{\text{MERR}}$, $\overline{\text{MRTY}}$) are driven inactive for one clock before being released.
 3. $\overline{\text{MBB}}$ is driven high for half clock cycle before being released.

Figure 3. MBus Single Read

MBus Single Write

Single write operations are queued in the store buffer. As soon as the module receives a bus grant, the transactions will be issued on the bus. The processor will not wait during this time, unless the buffer fills. Bytes, half-words, words, and double words may all be stored, with big-endian ordering. Any errors are reported as deferred data store errors. Figure 2 shows an MBus single write operation.

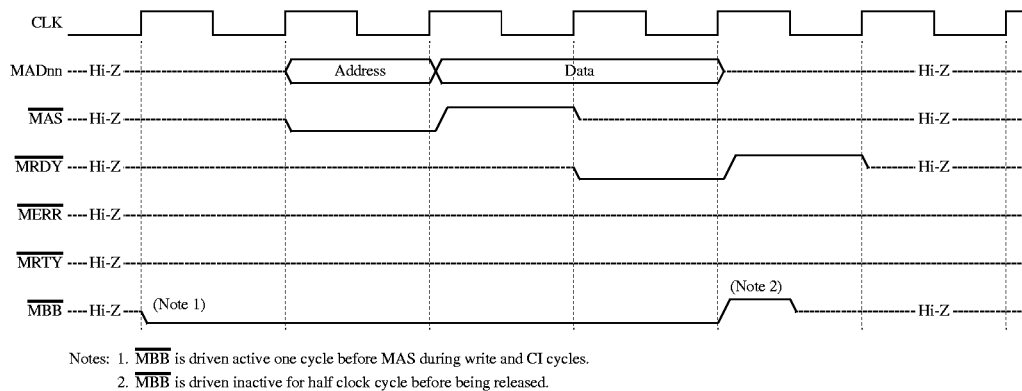
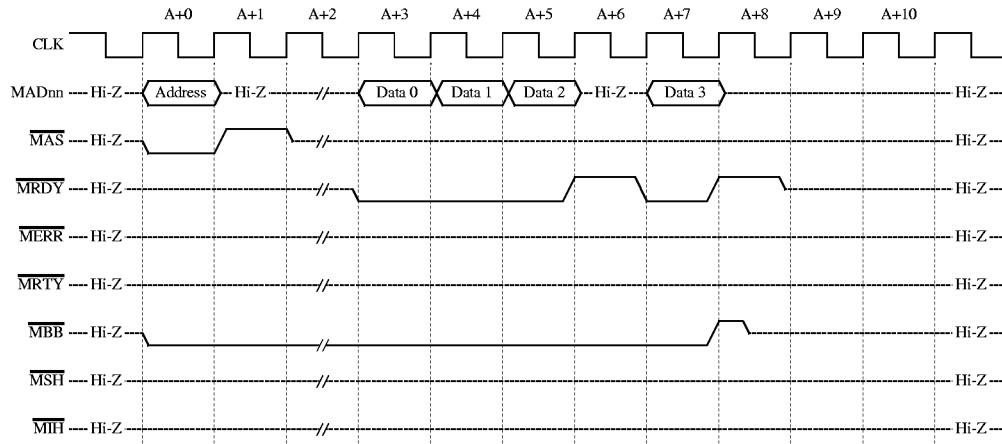


Figure 4. MBus Single Write

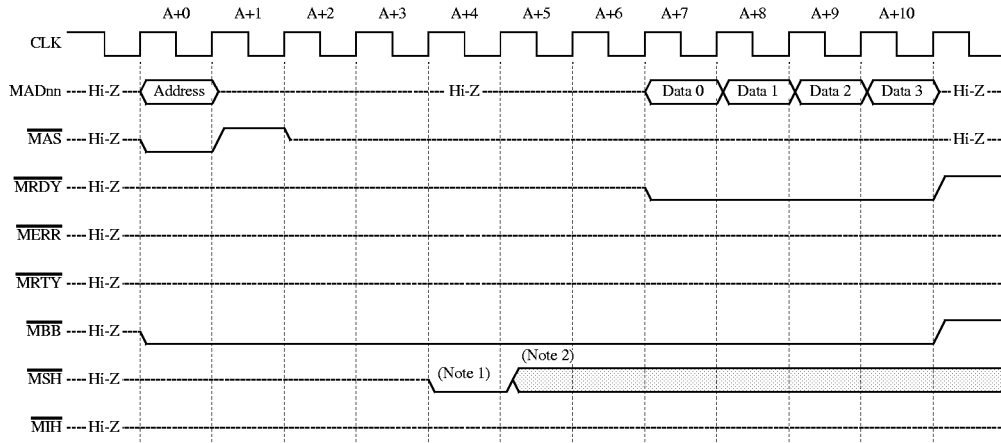
MBus Burst Read

Figure 3 shows a 32-byte burst read operation. A read operation can be performed on any size of data transfer that is specified by the SIZE bits. Read transactions support wrapping (critical-word- first ordering). Transactions involving fewer than eight bytes will have undefined data on the unused bytes.

**Figure 5. MBus Burst Read****MBus Coherent Read**

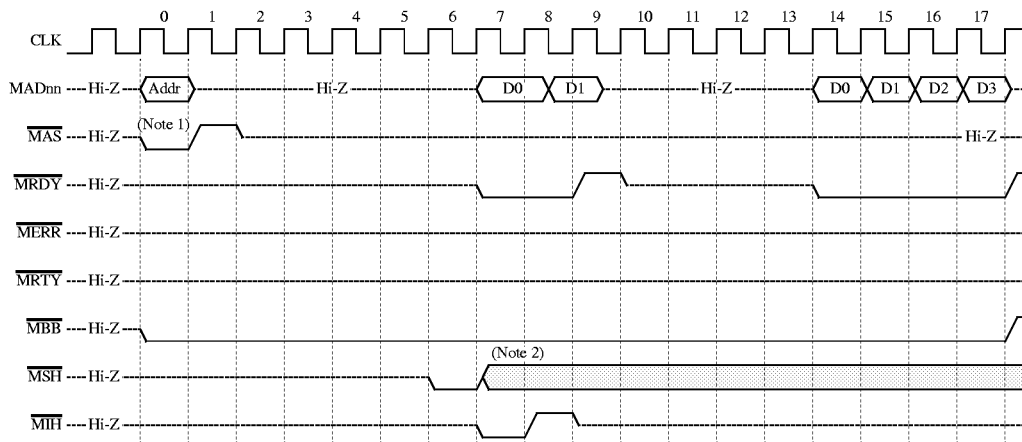
Coherent Read (CR) transactions are used to read data from the current owner. The owner may be memory or another cache. CR will be used for all on-board data cache load misses and all on-board instruction cache misses. If another cache owns the data, it will respond by asserting the $\overline{MIH}$ signal and providing the data. All CR transactions use critical-word-first ordering. The double-word that is needed first will be the starting address of the transaction. Double-words from memory must be returned in modulo 32-byte address order. Once the needed data arrives, the processor will use it immediately. Figure 4 shows an MBus coherent read of shared data. Any processor that has a valid cached copy of data referenced by CR transactions must assert the $\overline{MSH}$ signal to indicate that the information is shared. The module can accept the assertion of $\overline{MSH}$ at any time until receipt of the first data word. If the data is owned by another cache, the module will ignore any data ready responses until four cycles beyond the assertion of $\overline{MIH}$. This allows memory controllers to begin transmitting data sooner. Memory control-

lers must not respond with data until a time equal to the maximum $\overline{\text{MIH}}$ assertion delay for any cache in the system. Figure 5 shows an MBus coherent read of owned data.



- Notes: 1. $\overline{\text{MSH}}$ may occur from A+2 to A+7.
2. $\overline{\text{MSH}}$ is an open drain signal. It is not driven inactive. The system pull-up resistor returns it to an inactive level.

Figure 6. MBus Coherent Read of Shared Data



- Notes: 1. Device is not the Master.
2. $\overline{\text{MSH}}$ is an open drain signal. It is not driven inactive. The system pull-up resistor returns it to an inactive level.

Figure 7. MBus Coherent Read of Owned Data

MBus Coherent Invalidate

A Coherent Invalidate (CI) operation can only be performed on a block (32 bytes). All CI operations will be snooped by all snooping caches. If a Coherent Invalidate operation hits in a cache, that copy will be invalidated immediately, regardless of its state. Memory is responsible for the acknowledgment of the CI transaction. Figure 6 shows a CI operation.

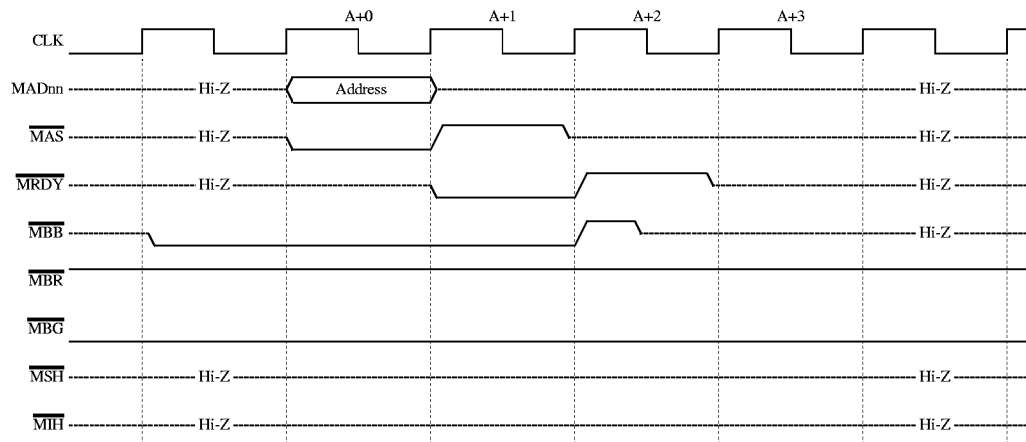


Figure 8. MBus Coherent Invalidate

Coherent Read and Invalidate

Since the MBus supports a write-invalidate type of cache-consistency protocol, a special Coherent Read and Invalidate (CRI) transaction that combines a CR transaction with the CI transaction was included to reduce the number of MBus Coherent transactions. Caches that are performing CR transactions with the knowledge that they intend to immediately modify the data can issue this transaction.

Each CRI transaction will be snooped by all system caches. If the address hits and the cache does not own the block, that cache immediately invalidate its copy of this block, no matter what state the data was in. If the address hits and the cache owns the block, the block will assert $\overline{MHI}$ and supply the data. When the data has been successfully supplied, the cache will then invalidate its copy of this block.

$\overline{MSH}$ is not driven during the CRI transaction.

Coherent Write and Invalidate

A Coherent Write and Invalidate transaction combines a block write transaction with a CI transaction.

Each Coherent Write and Invalidate transaction will be snooped by all system caches. If the address hits, caches will invalidate their copies of this block, no matter what state the data was in. Neither $\overline{\text{MIH}}$ nor $\overline{\text{MSH}}$ is asserted for Coherent Write and Invalidate transactions. Figure 7 shows a Coherent Write and Invalidate operation.

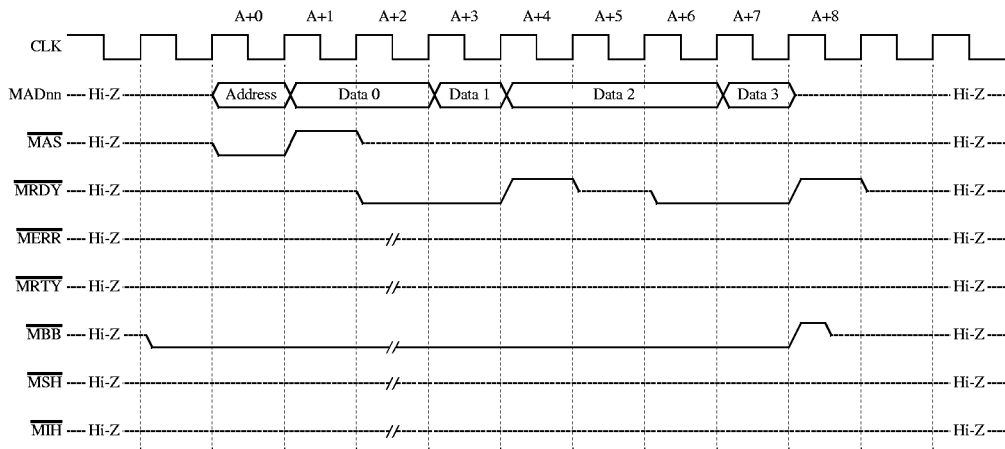


Figure 9. MBus Coherent Write and Invalidate

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings^[1]

Symbol	Parameter	Rating	Units
V _{CC}	Supply voltage range	0 to 6	V
V _I	Input voltage range	-0.5 to V _{CC} + 0.5	V
V _O	Output voltage range	-0.5 to V _{CC} + 0.5	V
I _{IK}	Input clamp current (V _I < 0 or V _I > V _{CC})	±20	mA
I _{OK}	Output clamp current (V _O < 0 or V _O > V _{CC})	±50	mA
	Current into any output in the low state	96	mA
T _{STG}	Storage temperature	-65 to 150	°C

1. Operation of the device at values in excess of those listed above will result in degradation or destruction of the device. All voltages are defined with respect to ground. Functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute -maximum-rated conditions may affect device reliability.

Recommended Operating Conditions

Symbol	Parameter		Min	Typ	Max	Units
V _{CC}	Supply voltage		4.75	5.0	5.25	V
V _{SS}	Ground		—	0	—	V
V _{IH}	Input high voltage		2.0	—	V _{CC} + 0.3	V
			2.2	—	V _{CC} + 0.3	V
V _{IL}	Input low voltage		-0.3	—	0.8	V
I _{OH}	Output high current		—	—	-2.0	mA
I _{OL}	Output low current	All outputs except $\overline{\text{MSH}}$	—	—	2.2	mA
		$\overline{\text{MSH}}$	—	—	8.0	mA
T _A	Operating ambient temperature		0	—	40 ^[1]	°C

1. Maximum ambient temperature indicates that the maximum junction temperature T_J of 85°C is not exceeded in the STP1020As and 80°C in the STP1090As when they are consuming maximum power (2 x 12.1 Watts by STP1020As, and 2 x 6 Watts by STP1090As) with air flow of 300LFPM at 10,000 feet altitude.

Power Consumption

This DVERO SuperSPARC module has a two built-in discrete regulators (one for each STP1020A) and they can operate with a $5.0\text{ V} \pm 5\%$ input power supply. The output of the regulators is $5.0\text{ V} \pm 50\text{mV}$. The worst case power consumption measured at 5.25 V, 50 MHz of VBus operating frequency is 55 Watts. This includes the worst case CPU power, the inefficiency of the regulators themselves driving the CPUs, worst case MXCC power, and the SRAM power. The I_{CC} given in the DC Characteristics is measured at the input to the module. The power consumptions is dependent of the software running. Power consumption with a typical application will be close to 75% of the worst case.

DC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OH}	Output high voltage ^[1]	$I_{OH} = \text{Max}, V_{CC} = \text{Min}$	2.4	–	–	V
V_{OL}	Output low voltage	$I_{OL} = \text{Max}, V_{CC} = \text{Max}$	–	–	0.4	V
I_{CC}	Supply current	$V_{CC} = 5.25, V_{BUS} = 50$ MHz, MBus = 40 MHz $t_{w(VCLK)}$ or $t_{w(CLK)} = \text{Min}$	10.5	–	11.6 ^[2]	A
I_{CCQ}	Quiescent power supply current	$V_{CC} = \text{Max}, V_I = V_{SS}$ or V_{CC}	–	425	–	mA
I_{OZ}	High-impedance output current	$V_{CC} = \text{Max}, V_O = 2.4\text{V}$	–	–	20	μA
		$V_{CC} = \text{Max}, V_O = 0.4\text{V}$	–	–	-20	μA
I_I	Input current	$V_I = V_{SS}$ to V_{CC} , Inputs with pullups	–	–	250	μA
		$V_I = V_{SS}$ to V_{CC} , All other inputs	–	–	50	μA
C_I	Input capacitance ^[3]		–	15	–	pF
C_O	Output capacitance ^[3]		–	25	–	pF

1. Open drain pins $\overline{\text{AERR}}$ and $\overline{\text{MSH}}$ not driven high.

2. The module power consumption includes the two STP1020As, the regulators inefficiency driving STP1020As only, the two STP1090As, and the SRAMs ($2 \times 12.1 + 2 \times 3.02 + 2 \times 6.0 + 2 \times 8 \times 0.8 = 55.04$; $55.04 / 4.75 = 11.6\text{ A}$).

3. This specification is provided as an aid to board design. This specification is not assured during manufacturing testing.

Timing Specification

This section provides the timing specifications of the MBus. All Mbus signals are TTL level signals. The signals should be measured at Low = 0.8V, and High = 2.0V. The threshold for clock is 1.5V for the purposes of making timing measurements and calculations. For timing purpose the Mbus signal are grouped in the following manner.

Bussed control signals: $\overline{MBB}$, $\overline{MAS}$, $\overline{MERR}$, $\overline{MRTY}$, $\overline{MRDY}$, $\overline{MIH}$, $\overline{MSH}$.

Address/ Data lines: MAD<63:00>.

Point to Point control signals: $\overline{MBR}$, $\overline{MBG}$.

MID[3:1] are static signal and have no specified timing. MIRL[3:0], AERR are asynchronous signals. $\overline{MSH}$ and $\overline{AERR}$ are open drain signals.

AC Characteristics: Module Timing - Setup and Hold

Symbol	Parameter	Signals	40 MHz MCLK		Unit
			Min	Max	
$t_{su}(MAD)$	MBus MAD lines setup to CLK	MAD[63:0]	3.9	—	ns
$t_{su}(MC)$	MBus bused setup to CLK	$\overline{MAS}$, $\overline{MERR}$, $\overline{MRTY}$, $\overline{MRDY}$, $\overline{MBB}$, $\overline{MSH}$, $\overline{MIH}$	5.0	—	ns
$t_{su}(MIRL)$	MBus IRL[3:0] setup to CLK	IRL[3:0]	5.0	—	ns
$t_{su}(MBG)$	MBus point-to-point setup to CLK	$\overline{MBG}$	6.8	—	ns
$t_h(MAD)$	MBus MAD lines hold from CLK	MAD[63:0]	3.5	—	ns
$t_h(MC)$	MBus bused hold from CLK	$\overline{MAS}$, $\overline{MRDY}$, $\overline{MBB}$, $\overline{MERR}$, $\overline{MRTY}$, $\overline{MSH}$, $\overline{MIH}$, IRL[3:0]	3.5	—	ns
$t_h(MBG)$	MBus Point-to-point hold from CLK	$\overline{MBG}$	3.5	—	ns

AC Characteristics: Module Timing - Switching Characteristics^{[1] [2]}

Symbol	Parameter	40 MHz MCLK		Unit
		Min	Max	
$t_p(MAD)$	Propagation delay, CLK to MBus MAD[63:0]	—	17.3	ns
$t_p(MC)$	Propagation delay, CLK to MBus control $\overline{MAS}$, $\overline{MRDY}$, $\overline{MBB}$, $\overline{MIH}$, $\overline{MSH}$	—	17.7	ns
$t_p(MBR)$	Propagation delay, CLK to MBus point-to-point $\overline{MBR}$	—	16.4	ns
$t_{oh}(MAD)$	Output hold time, CLK to MBus MAD[63:0]	3.5	—	ns
$t_{oh}(MC)$	Output hold time, CLK to MBus control $\overline{MAS}$, $\overline{MRDY}$, $\overline{MBB}$, $\overline{MIH}$, $\overline{MSH}$	4.5	—	ns
$t_{oh}(MBR)$	Output hold time, CLK to MBus point-to-point $\overline{MBR}$	4.6	—	ns

1. Timing specification are based on a lumped capacitive load of 50pf.
2. Timing specifications are based on Spice simulations.

Clock Timing^[1]

Symbol	Parameter	Min	Typ	Max	Unit
t _w (MBUS CLK)	MBus CLK pulse duration (40 MHz)	25	–	–	ns
	MBus CLK duty cycle	25	50	75	%
t _w (SCAN CLK)	SCAN CLK pulse duration (10 MHz)	100	–	–	ns
	SCAN CLK duty cycle	–	50	–	%

1. This is for the PLL enabled. If the PLL is disabled, the part supports a fully static design. The timing parameters are not assured, since this is not tested.

JTAG and Miscellaneous Timing - Setup and Hold

Symbol	Parameter	Signal	10 MHz		Unit
			Min	Max	
t _{su} (SCAN TRST)	Setup to VCLK	$\overline{\text{SCANTRST}}$ (synchronous) ^[1]	20	–	ns
t _{su} (SCAN DI)	JTAG setup to SCAN CLK	SCANDI	20	–	ns
t _{su} (SCANTMS)	JTAG setup to SCAN CLK	SCANTMS	20	–	ns
t _h (SCAN TRST)	Hold from VCLK	$\overline{\text{SCANTRST}}$ (synchronous) ^[1]	20	–	ns
t _h (SCAN DI)	JTAG hold from SCAN CLK	SCANDI	20	–	ns
t _h (SCANTMS)	JTAG hold from SCAN CLK	SCANTMS	20	–	ns

1. SCAN RESET can occur anytime during a clock cycle. Time given is minimum to ensure synchronous operation.

JTAG and Miscellaneous Timing - Switching Characteristics

Symbol	Parameter	Min	Max	Unit
t _p (SCANDO)	SCAN CLK (falling edge) to SCANDO	2.5	20	ns

MECHANICAL SPECIFICATIONS

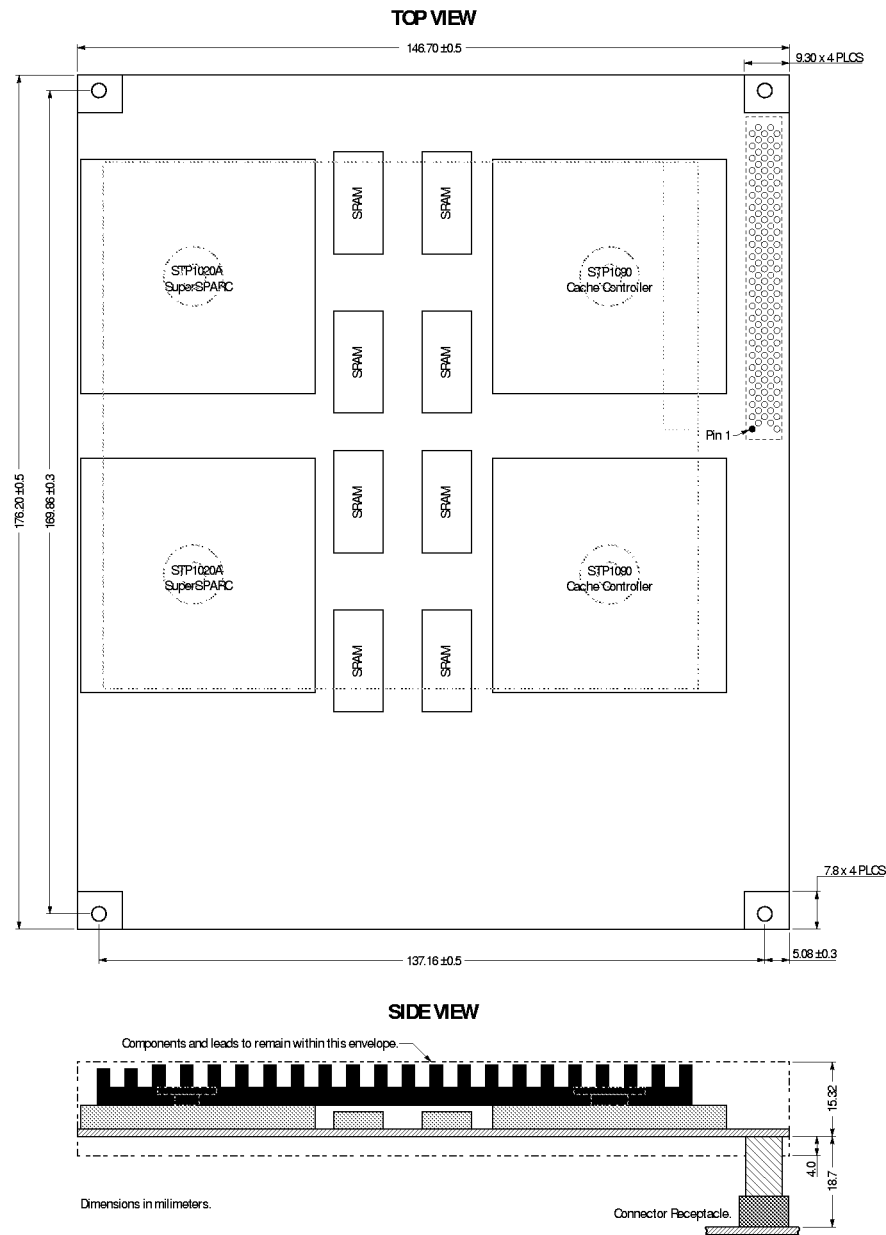
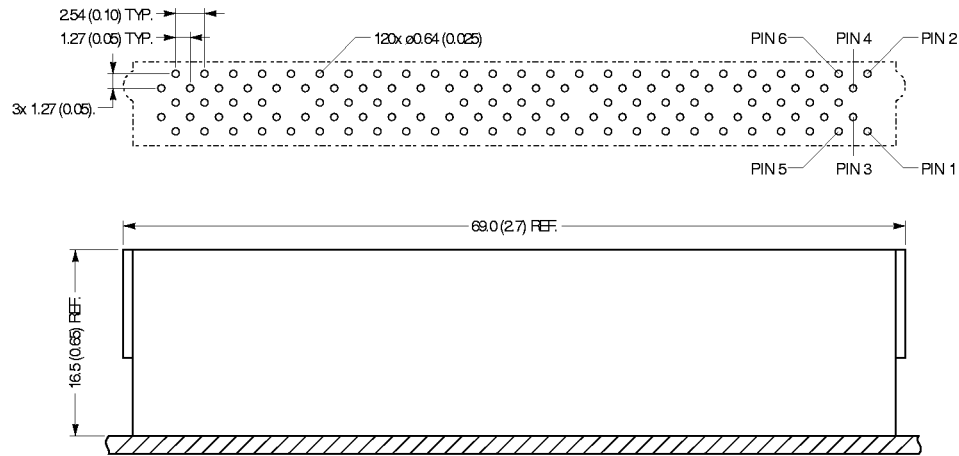


Figure 10. CPU Module Dimensions



Notes: 1. Dimension in Inches. Dimensions in parenthesis in mm.
2. Connector part number: AMP 121354-4 or Fujitsu MCN-264P100-G/C.
3. For complete connector specifications, contact the manufacturer.

Figure 11. CPU Module Connector (Detail Drawing)

ENVIRONMENTAL, SHOCK, & VIBRATION SPECIFICATION

Parameter	Specification
Operating Humidity	5% to 95% RH
Nonoperating Humidity	95% RH
Operating Altitude	63kPa, 10 C to 40 C
Nonoperating Altitude	17.3kPa, 0 C
Operating Shock	6 G, 11 msec, half-sine, 10 impacts/face
Nonoperating Shock	35 G, 11 msec, half-sine, 3 impacts/face
Operating Vibration	0.3 G peak, 2 sweeps of 5 to 500 to 5 Hz
Nonoperating Vibration	1.2 G peak, 2 sweeps of 5 to 500 to 5 Hz

The following additional test are performed during Engineering Qualification.

Parameter	Specification
Operating Temp. Soak Test	-5 C to 75 C, 20 C/min., 8 hrs. at each extreme.
Nonoperating Temp Soak Test	-40 C to 125 C, 20 C/min., 8 hrs at each extreme.
Operating Temp. Cycle Test	Twenty cycles of 0 to 60 °C, 20 °C / min., with ten minutes of dwell at 0 °C and 60 °C respectively.
Non-operating Temp. Cycle Test	Twenty cycles of -40 to 90 °C, 20m°C/min, with ten minutes of dwell at -40 °C and 90 °C respectively.
Non Operating Tri-Axial Random Vibration 20 to 2 kHz bandwidth	- 25 GRMS measured at center of test board for 10 minutes at 40, 25 and 85 °C
Operating Tri-axial Random Vibration 20 to 2 kHz bandwidth	- 25 GRMS measured at center of test board for 10 minutes at 0, 25 and 60 °C
Power Cycling tests	Apply voltage for 5 seconds on and 5 seconds off during twenty cycles of 0 to 60 °C, 20 °C/min., with five minutes of dwell at 0, 25 and 60 °C respectively.
Solder Reliability Tests	Non powered temperature cycling of 0 to 100 °C, 20 °C per minute change rate, 10 minute dwells at 0 °C and 100 °C, for 1000 cycles.

Note: The temperature and vibration, values and methodologies are derived from a combination of industrial component manufacture tests, Mil-Std 883 tests, IEC Tests, and from tests performed in Sun's Stress Lab.



Thermal Resistance vs. Air Flow ^[1] ^[2]

Symbol	Air Flow (ft./min)				
	100	200	300	400	500
θ_{CA} (°C/W)	6.5	5.2	4.5	4.0	3.7

1. T_J can be calculated by: $T_J = T_A + P_d(0.6 + \theta_{CA})$. Maximum T_J for STP1020A is 105 °C.
2. The above θ_{CA} values are with pin-fin-type heat-sink.

Dual SuperSPARC + E-Cache Module - Dual 50 MHz SuperSPARC MBus Module™

Preliminary
STP5022B

ORDERING INFORMATION

Part Number	Speed	Description
STP5022BMBUS-50	50 MHz VBUS, 40 MHz MBus	50 MHz VBUS, 40 MHz MBus module with two STP1020As, two STP1090As, a total of 2 MB E-Cache, two 50 MHz Clocks, two Discrete Voltage Regulators.