UltraSPARC® IIi at 550/650 MHz

Addendum to UltraSPARC IIe User's Manual

Version 1.1

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CHAPTER 1

Introduction

This addendum contains information about the differences between the UltraSPARC® IIi processor at 550/650 MHz from the UltraSPARC IIe processor at 400/500 MHz. This addendum also references the UltraSPARC IIe User's Manual.

Topics
- Overview
- Power Management – Energy Star Mode
- Level 2 Cache
- Memory Controller Unit

Related Material
- UltraSPARC IIe User's Manual

1.1 Overview

The UltraSPARC IIi processor at 550/650 MHz is pin and package-compatible with the UltraSPARC IIe processor at 400/500 MHz. The UltraSPARC IIi processor implements a 64-bit, SPARC V9 architecture with the VIS™ instruction set. The UltraSPARC IIi device technology and design enables high levels of integration; the processor includes an SDRAM memory controller, a PCI Bus interface, on-chip 512 KB of L2-cache, and power management features. TABLE 1-1 outlines the differences between the UltraSPARC IIe and UltraSPARC IIi processors.

TABLE 1-1 UltraSPARC IIe and UltraSPARC IIi Processors – Notable Differences

Features	UltraSPARC IIe (400/500 MHz)	UltraSPARC IIi (550/650 MHz)
Sun Platforms	Sun Blade™ 100, Netra™ t1120/5, t1400/5, CP2060/2080, AX1105	Sun Blade 150, Sun Fire™/Netra v120, Sun Fire v100
Clock Frequency	400/500 MHz	550/650 MHz
Energy Star Modes	1/2, 1/6 operating frequency	1/2, 1/4, 1/6, and 1/8 operating frequency
Level-2 Cache Size, Associativity	256 KB, 4-way	512 KB, 4-way
Max. Memory Space	2 GB	4 GB

TABLE 1-1 UltraSPARC IIe and UltraSPARC IIi Processors – Notable Differences *(Continued)*

Features	UltraSPARC IIe (400/500 MHz)	UltraSPARC IIi (550/650 MHz)
SDRAM Device Support	Up to 256 Mb	Up to 512 Mb
Programmable SDRAM Features	No	Yes
Process Technology	0.18 micron, Aluminum	0.18 micron, Copper

CHAPTER **2**

Power Management - Energy Star Mode

The UltraSPARC IIi processor enhances the UltraSPARC IIe processor's power management features by supporting additional Energy Star (E-Star) modes. The UltraSPARC IIi processor can be slowed to 1/2, 1/4, 1/6, and 1/8 the normal operating frequency to reduce power consumption. The following figure and table is a revised version of *Table 2-1: Energy Star Register Data Field* in *Chapter 2: Clocks, System Timer, GPO, and Resets, page 15* of the UltraSPARC IIe User's Manual.

E-Star Register Data Field Read/write: 0x01FE.0000.F080

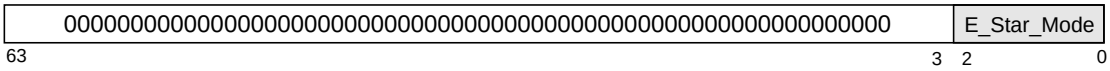

FIGURE 2-1 Energy Star Register Data Field

TABLE 2-1 Energy Star Registration Data Fields

Field	Bits	Description	POR	Type
Reserved	63:3	Reserved	–	–
E_Star_Mode	2:0	• 000: Full operating frequency • 001: 1/2 operating frequency • 011: 1/4 operating frequency • 010: 1/6 operating frequency • 100: 1/8 operating frequency • 101, 110, 111: Reserved	000	R/W

Note – There are no changes to the address map for the E-Star mode and stick registers.

CHAPTER **3**

Level 2 Cache

The Level 2 cache (L2-cache) in the UltraSPARC IIi processor is 512 KB (twice the size of the UltraSPARC IIe processor) and 4-way set-associative. The following modifications to the L2-cache for the UltraSPARC IIi references *Chapter 3: Level 2 Cache Subsystem* of UltraSPARC IIe User's Manual.

3.1 UPA Configuration Register

In *Table 2: UPA_Config Register Data Fields, page 67*, `elim` (bits 35:33) is read as 101 on POR.

3.2 Tag RAM Diagnostics Address Register

The tag RAM diagnostics register, shown on *page 34* of the UltraSPARC IIe User's Manual, reflects an L2-cache size of 256 KB. Since the UltraSPARC IIi features a 512 KB of L2-cache, FIGURE 3-1 reflects the modified tag RAM diagnostics register:

L2-Cache Tag RAM Diagnostics Address Register

Read: ASI_ECACHE_R (0x07E)
Write: ASI_ECACHE_W (0x076)

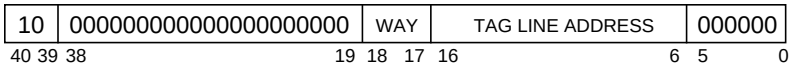

FIGURE 3-1 L2-Cache Tag RAM Diagnostics Address Register

3.3 Tag RAM Diagnostics Data Field

The tag RAM diagnostics data field, shown on *page 34* of the UltraSPARC IIe User's Manual, reflects an L2-cache size of 256 KB. Since the UltraSPARC IIi features a 512 KB of L2-cache, FIGURE 3-2 reflects the modified tag RAM diagnostics data field:

L2-Cache Tag RAM Diagnostics Data Field

Read: ASI_ECACHE_R (0x04E)
Write: ASI_ECACHE_W (0x04E)

Note: Bits [63:22] are not physically implemented. These bits return zero when accessed.

Note: This RAM entry is logically part of the tag/valid RAM array and the *rand* RAM array.

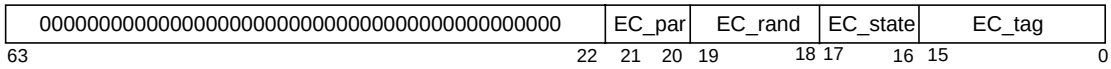

FIGURE 3-2 L2-Cache Tag RAM Diagnostics Data Field

The revised fields, bits, and other descriptions are shown in TABLE 3-1.

TABLE 3-1 L2-Cache Tag RAM Diagnostics Data Field

Field	Bit(s)	Description	POR	Type
Reserved	63:22	Reserved	Unknown	RZ
EC_par	21	EC_state[17:16], and EC_tag[15:9] Parity	Unknown	R/W
	20	EC_tag<8:0> Parity	Unknown	R/W
EC_rand	19:18	2-bit L2-cache rand field to support random way selection for allocation in 4-way set associative mode	Unknown	R/W
EC_state	17:16	• 00: Invalid Entry (line available) • 01: Reserved • 10: Exclusive (valid, unmodified) • 11: Modified (valid, modified)	Unknown	R/W
EC_tag	15:0	Physical Address [31:16] tag	Unknown	R/W

3.4 Data RAM Diagnostics Register

The data RAM diagnostics register, shown on *page 35* of the UltraSPARC IIe User's Manual, reflects an L2-cache size of 256 KB. Since the UltraSPARC IIi features a 512 KB of L2-cache, FIGURE 3-3 reflects the modified data RAM diagnostics register:

L2-Cache Data RAM Diagnostics Virtual Address

Read: ASI_ECACHE_R (0x07E)
Write: ASI_ECACHE_W (0x076)

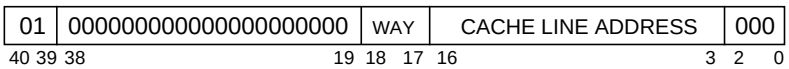

FIGURE 3-3 L2-Cache Data RAM Diagnostics Virtual Address

CHAPTER 4

Memory Controller Unit

The UltraSPARC IIi processor supports up to 4 GB of main memory and supports 512 Mb SDRAM devices. TABLE 4-1 shows the possible configurations.

TABLE 4-1 SDRAM Parameters for 512 Mb DIMM Configurations

Base SDRAM Device Configuration		Number of Devices per Side	Capacity per Side	Mem_Control_2: DIMM_x_SDRAM_Size	
				[15:14]	[13:12]
512 Mb	32Mx16	5	256 MB	00	00
	64Mx8	9	512 MB	01	00
	128Mx4	18	1 GB	10	00

TABLE 4-2 reflects the modified (changes shown as highlighted) Processor Subsystems Memory Mapped CSRs on page 41 of the UltraSPARC IIe User's Manual.

TABLE 4-2 Processor Subsystems Memory Mapped CSRs

Address PA<40:0>	Description	Destination
0x1FE.0000.F000	FFB.Config (no UPA64s)	L2-cache
0x1FE.0000.F008	Reserved	
0x1FE.0000.F010	Mem_Control_0 (MC0)	MCU
0x1FE.0000.F018	Mem_Control_1 (MC1)	MCU
0x1FE.0000.F020	Reset Control	PIE
0x1FE.0000.F028	Mem_Control_2 (MC2)	MCU
0x1FE.0000.F030	Mem_Control_3 (MC3)	MCU
0x1FE.0000.F038	Reserved	
0x1FE.0000.F040	General Purpose Mode Register	GPIO
0x1FE.0000.F048	General Purpose Output Register	GPIO
0x1FE.0000.F050	General Purpose Input Register	GPIO
0x1FE.0000.F058	Reserved	
0x1FE.0000.F060	Stick_Cmp_Low	STICK
0x1FE.0000.F068	Stick_Cmp_High	STICK

TABLE 4-2 Processor Subsystems Memory Mapped CSRs *(Continued)*

Address PA<40:0>	Description	Destination
0x1FE.0000.F070	Stick_Reg_Low	STICK
0x1FE.0000.F078	Stick_Reg_High	STICK
0x1FE.0000.F080	E-Star_Mode	CCU

4.1 Memory Control 0 Register: Timing and Control

TABLE 4-3 Memory Control 0 Register Bit Definitions; Timing and Control

Register Name	Description	Register Address	POR Reset Value
Memory_Control_0 MC0	Timing and control	1FE.0000.F010	32'h77B0_0286

Register Field	Symbol	Bits	Description	POR	Type
Clock_Ratio [1]		31:29	Processor to SDRAM clock ratio: 000 = 4 to 1 001 = 5 to 1 010 = 6 to 1 011 = 7 to 1 100 = 8 to 1 101 = 9 to 1 110 = Reserved 111 = Reserved	101	R/W
T_{RAS}	RAS	28:26	RAS Active to Precharge Time. 3 to 6 SDRAM clocks. 000 = Reserved 010 = Reserved 011 = 3 100 = 4 101 = 5 110 = 6 111 = Reserved	101	R/W
T_{RP}	RP	25:24	Precharge Command Period. 2 or 3 SDRAM clocks.	11	R/W
T_{WR}	WR	23:22	Write Recovery Time. 1 or 2 SDRAM clocks.	10	R/W
T_{RCD}	RCD	21:20	RAS to CAS Delay. 2 or 3 SDRAM clocks.	11	R/W
Reserved		19:18		00	RO
DIMM_Registered		17	DIMM type: 0 = Unregistered, 1 = Registered	0	R/W
Self_Refresh		16	SDRAM Self Refresh Enable 0 = Disabled, 1 = Enabled	0	R/W
Auto_Refresh		15	Enables the MCU to perform SDRAM refreshes at the specified refresh intervals. 0 = Disabled, 1 = Enabled	0	R/W

Register Field	Symbol	Bits	Description	POR	Type
Refresh_Intervals		14:8	Interval between MCU initiated refreshes. Each encoding is 64 processor clocks. The E-Star mode setting affects the processor clock frequency.	0000010	R/W
Enable_ECC		7	All ECC functions. 0 = Disabled, 1 = Enabled	1	R/W
Reserved		6:4		0	R/W
T_{CL}	CL	3:1	CAS Latency. 010 = 2 SDRAM clocks, 011 = 3 SDRAM clocks, All others Reserved.	011	R/W
MRS_Initiate		0	Software must transition this bit from a low to a high to initiate the hardware to write the MRS value to the SDRAMs. This bit can be left as 1 or be immediately returned to a 0.	0	R/W

1. The Clock_Ratio field should only be programmed once during initialization to a value that maximizes SDRAM clock frequency for a given processor clock frequency within the PC-100 limit. Switching the Clock_Ratio bits during normal operation is prohibited.

4.2 Memory Control 2 Register

The 4 DIMM chip select base address fields in Memory Control Register 1 have been expanded to 9 bits using reserved space in Memory Control Register 2 to support the larger 4 GB memory space.

The DIMM CS base address value must be split between two register fields. The lower 8 bits remain in the Memory Control Register 1. The 9th bits for each bank are in the Memory Control Register 2 and are shown in TABLE 4-4.

TABLE 4-4 Memory Control 2 Register Bit Definitions: Miscellaneous

Register Field	Bits	Description	POR	Type
DIMM_3_CS_Addr[8]	31	9th bit of Memory Control Register 1 field for DIMM 3.	0	R/W
DIMM_2_CS_Addr[8]	30	9th bit of field for DIMM 2.	0	
DIMM_1_CS_Addr[8]	29	9th bit of field for DIMM 1.	0	
DIMM_0_CS_Addr[8]	28	9th bit of field for DIMM 0.	0	
DIMM_3_SCLK_Enable	27	Enable MEM_SCLK3, 7 to operate. 0 = Disabled, no activity 1 = Enabled, clock is active	0	R/W
DIMM_2_SCLK_Enable	26	Enable MEM_SCLK2, 6 to operate.	0	R/W
DIMM_1_SCLK_Enable	25	Enable MEM_SCLK 1, 5 to operate.	0	R/W
DIMM_0_SCLK_Enable	24	Enable MEM_SCLK 0, 4 to operate.	0	R/W
DIMM_3_Present	23	Occupied DIMM slot 3. 0 = Empty, 1 = Populated	0	R/W

TABLE 4-4 Memory Control 2 Register Bit Definitions: Miscellaneous *(Continued)*

Register Field	Bits	Description	POR	Type
DIMM_2_Present	22	Occupied DIMM slot 2.	0	R / W
DIMM_1_Present	21	Occupied DIMM slot 1.	0	R / W
DIMM_0_Present	20	Occupied DIMM slot 0.	0	R / W
DIMM_3_Double	19	Double Sided DIMM in slot 3 has two physical banks of SDRAMs on it. 0 = Single sided (banked) DIMM 1 = Double sided (banked) DIMM	0	R / W
DIMM_2_Double	18	Double Sided DIMM in slot 2.	0	R / W
DIMM_1_Double	17	Double Sided DIMM in slot 1.	0	R / W
DIMM_0_Double	16	Double Sided DIMM in slot 0.	0	R / W
DIMM_3_SDRAM_Size[1]	15:14	Size of SDRAM devices on DIMM 3 TOTAL SIZE: 00xxh = 16 Mb 01xxh = 64 Mb 10xxh = 128 Mb 11xxh = 256 Mb	0x0	R / W
	13:12	WIDTH: xx00h = Reserved xx01h = By 16 bits xx10h = By 8 bits xx11h = By 4 bits	0x0	R / W
DIMM_2_SDRAM_Size	11:8	Size of SDRAM devices on DIMM 2.	0	R / W
DIMM_1_SDRAM_Size	7:4	Size of SDRAM devices on DIMM 1.	0	R / W
DIMM_0_SDRAM_Size	3:0	Size of SDRAM devices on DIMM 0.	0	R / W

1. The SDRAM size does not convey any information about the DIMM sizes. SDRAM size refers to the size and organization of the SDRAM devices used on the DIMM.

4.3 Memory Control 3 Register

TABLE 4-5 Memory Control Register 3 Bit Definitions

Field	Bit(s)	Description	Function	POR	Type
$T_{SDRAM\_CLOCK\_SHIFT}$[1]	31:28	Shifts the SDRAM clock output edge.	0000: No delay or advancement 0001: Delay 0.5 processor clocks 0010: Delay 1.0 0011: Delay 1.5 0100: Delay 2.0 0101: Delay 2.5 0110: Delay 3.0 0111: Reserved 1000: Reserved 1001: Advance 0.5 processor clocks 1010: Advance 1.0 1011: Advance 1.5 1100: Advance 2.0 1101: Advance 2.5 1110: Advance 3.0 1111: Reserved	0	R/W
$T_{DATAREAD\_SHIFT}$[2]	27:24	Shifts the input latch edge for read data.		0	R/W
$T_{COMMAND\_SHIFT}$[3] *(Phase Enable)*	23:21	Shifts the output signal edges for all the command signals and the Feedback Shift, too.	000: No delay or advancement 001: Reserved 010: Delay 2 processor clocks 011: Delay 1 100: Advance 1 processor clock 101: Advance 2 110: Reserved 111: Reserved	0	R/W
Clock_Div	20:19	Sets the processor clock divisor.	00: Divide processor clock by 4 01: Divide processor clock by 2 10: Divide processor clock by 2 11: Divide processor clock by 1	0	R/W
Reserved	18:15	Reserved		0	
SDRAM Control Delay B	14	The delay for the SDRAM control signals associated with address bus B. 0 = On POR 1 = Add delay		0	R/W
BIST_Error	13	Asserts when the BIST logic detects an error.		0	R/W
BIST_Done	12	Asserts when the BIST logic is done testing the processor.		0	R/W

TABLE 4-5 Memory Control Register 3 Bit Definitions *(Continued)*

Field	Bit(s)	Description	Function	POR	Type
IO_Data[0]	11	Holds the value of the Data bus bit [0] after BIST.		0	R/W
SDRAM Control Delay A	10	The delay for the SDRAM control signals associated with address bus A: MEM_CLKE, MEM_RAS_L, MEM_CAS_L, MEM_WE_L. 0 = On POR 1 = Add delay		0	R/W
Buffer Strengths	9:0	Sets the DC current drive strengths of the output buffers for the command signals.	See the Memory Control Register 3 definition in the UltraSPARC IIe User's Manual.	0	R/W

1. The SDRAM clock can be shifted relative to the command strobes in 1/2 processor clock increments.
2. Timing to latch the data read from the SDRAMs. This value can be used to adjust set-up and hold timing into the processor. The latching edge can be shifted in 1/2 processor clock increments.
3. The interface command shift moves the edges for the following signals: MEM_RAS, MEM_CAS, MEM_WE, MEM_CLKE, MEME_CS, MEM_READ_DATA_LATCH (internal).

Note – $\overline{T}_{SDRAM\_CLOCK\_SHIFT\ <31:28>}$ and $T_{DATAREAD\_SHIFT\ <27:24>}$ can only be adjusted for systems that would never go into E-Star mode. For systems in E-Star mode, these two control fields must be set at the default value.

$T_{COMMAND\_SHIFT\ <23:21>}$ is recommended to be set at 011.
