



SPARC64 V Microprocessor Provides Foundation for PRIMEPOWER Performance and Reliability Leadership

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ABOUT THIS DOCUMENT

This paper offers an overview of the key microprocessor-related features of PRIMEPOWER servers. It is one in a series of six white papers that highlight PRIMEPOWER hardware and software capabilities from a customer-benefits perspective. Additional information concerning PRIMEPOWER's SPARC64 V and other PRIMEPOWER technology can be found on the Fujitsu websites: www.fujitsu.com/global/services/computing/server/unix/.

Executive Summary

Fujitsu's SPARC64 V microprocessor is a fundamental building block that allows Fujitsu's PRIMEPOWER servers to deliver the highest levels of performance, availability, flexibility, scalability, and security. Although it is not necessary for the CIO or CTO to fully understand the details of Fujitsu's processor implementation, the microprocessor is a key element of advanced system design, and an overview of the chip's unique attributes will help explain the benefits found in the PRIMEPOWER servers. This paper offers such an overview.

While processor designers are understandably proud of the innovations they have incorporated into their latest chips and enjoy describing the deepest details of their designs – especially to system developers who certainly need to understand those specifics – customer IT executives may feel overwhelmed with this level of detail. Nonetheless, an appreciation of the element of processor innovation can highlight system differentiation.

Fujitsu's SPARC64 family of processors provides the underlying foundation that permits PRIMEPOWER to deliver leadership performance and reliability. This white paper reviews some of the unique capabilities designed into the SPARC64 and lays out benefits that would appeal to an IT executive. Hence, the paper avoids the level of detail needed by system developers.

For over fifty years, Fujitsu has honed its skills in advanced processor development. From its first commercial computer in 1954, through high-capacity mainframes and vector supercomputers, Fujitsu has created impressive high-end processors. Fujitsu has applied this design expertise to innovative SPARC implementations. Beginning in 1995, Fujitsu has been delivering 64-bit SPARC64 processors, compliant with the SPARC V9 specification. (See the sidebar, "An Open Standard for Microprocessors" for details.)

SPARC64 – Designed for Performance

Even though megahertz and gigahertz are popularly used as performance indicators, processor performance is not solely related to clock speed. Rather, increased performance derives from doing more work per clock cycle as well as speeding up the number of clock cycles per second.

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SPARC – AN OPEN STANDARD FOR MICROPROCESSORS

SPARC, an acronym for “Scalable Processor Architecture,” is an open-standard processor architecture overseen by a non-profit organization. SPARC licensees conform to the IEEE Standard SPARC instruction set, but maintain the freedom to tune their designs to best meet product needs, which may include embedding a processor within an appliance or powering a high-performance server.

Fujitsu was a founding member of SPARC International and a key contributor to the evolution of the specifications, especially the SPARC V9 extension, which provides full 64-bit support. In December 1995, Fujitsu’s SPARC64 was the first 64-bit SPARC V9 processor to be shipped. That initial SPARC64 chip was followed by other V9-compliant Fujitsu implementations that offered increased performance, among other features. The latest chip, SPARC64 V, offers high performance and RAS (reliability, availability, and serviceability) characteristics that set it apart from alternative SPARC implementations.

Software written to the SPARC V9 specification will be portable to any of the chip implementations. Thus, PRIMEPOWER systems can run the broad portfolio of applications that run on Sun’s UltraSPARC-based platforms. Some system-level programming may require optimization for particular chip implementations. For example, code may need to be modified to take advantage of the unique error-handling capabilities of SPARC64. Such platform-specific extensions are developed by Fujitsu and do not affect the ability to run SPARC-compliant applications.

The open SPARC specification permits implementation choices, as indicated in the sidebar. For example, users may incorporate circuitry that increases performance or enhances reliability. For SPARC64 V, Fujitsu has increased the instruction-level parallelism beyond that of other SPARC implementations. Specialized instruction decode and execution scheduling hardware analyzes data dependencies and potential instruction parallelism for code segments, allowing multiple execution units to remain busy in SPARC64’s out-of-order superscalar design.

Thanks in part to aggressive prefetching circuitry, up to six instructions may execute simultaneously. A large branch history table helps predict the outcome of multiple code branches as well as the destination addresses. Sizable on-chip caches – including a non-blocking, set-associative 4 MB on-chip L2 cache – and fast data paths (up to 69 GB/sec.) satisfy the execution units’ data needs. The effective wait for data from main memory is minimized by a non-blocking cache design, instruction execution initiated prefetch, and data prefetch triggered by cache miss prediction algorithms. Up to 16 out-of-order memory requests can be outstanding. The specific techniques involved are best appreciated by processor design practitioners, but the result that impresses IT executives is increased instruction execution per clock cycle, which, in turn, increases PRIMEPOWER performance in the enterprise computing environment.

State-of-the-art semiconductor technology can create chips with high clock frequency, but that is only one aspect of high-performance design. SPARC64 designers look to optimize the balance of work-per-clock and clocks-per-second. Entirely different chip architectures, such as the Pentium, may focus primarily on gigahertz and use that as their bragging point. Even for the open SPARC architecture, different chip designs may choose a different balance that puts more weight on clock rate. For example, past SPARC64 processors have offered high-end performance superior to UltraSPARC while employing around the same clock rates.

Nonetheless, in addition to more work per cycle, SPARC64 V also employs state-of-the-art 90 nm semiconductor technology to run at a 2 GHz clock rate. SPARC64 V has achieved 1,594 SPECint2000, which is the world’s fastest result among UNIX server processors.

Bragging rights for owning the fastest chip may delight a home PC user, but a CIO, CTO, or other IT executive is concerned about accomplishing the organization’s computing workload efficiently. Higher-performing processors mean more work can be done with fewer servers. That means less cost in running, managing, and maintaining the computing infrastructure. Fujitsu’s high-performance SPARC64 processors provide muscle that enables PRIMEPOWER to scale to meet the needs of the most demanding users.

SPARC64 – Designed for Reliability and Availability

SPARC64’s design emphasis of more work per clock cycle rather than excessive clock frequency carries the benefit of relatively lower power consumption. As clock rates increase, more electrical power is required to drive the chip circuitry. This increase in electrical power results in more heat being produced – and hotter chips suffer more failures.

SPARC64 is designed for high performance and not for the very low power consumption expected of embedded processors. Relative to other high-performance chips, SPARC64 consumes about 65 watts of power compared with over 100 watts for some competitors. By choosing a chip design point that does not require excessive clock speed, Fujitsu designers can create reliable platforms with dense, compact packaging, without the need for exotic, expensive cooling technology.

Picking a design point that delivers performance without excessive thermal dissipation provides a reliability advantage. But, even more important, the 90 nm process technology offers SPARC64 chip designers a large number of circuits not only to increase performance but also to directly enhance error detection for fault isolation. Compared with today's chip capabilities, early RISC chips had fewer circuits available on each piece of silicon. Designers typically focused on performance with less emphasis on error isolation.

From their mainframe design expertise, Fujitsu's processor engineers have extensive experience in designing error detection and correction circuits. The technology employed in high-end systems was far different in the mid-1970s when Fujitsu began designing mainframes. High-performance systems used technology with relatively few circuits per chip. The chips ran hot, which reduced reliability. Furthermore, interconnecting the thousands of chips needed for a mainframe required extensive wiring and connectors that had high failure rates. As a consequence, mainframe designers developed elaborate error checking circuitry to detect and isolate failures.

Hardware instruction retry was a technique used in mainframes beginning in the 1970s. Many error conditions are intermittent and the failing instruction can be re-executed successfully, as long as proper machine-state has been saved. This retry mechanism allows SPARC64 to back up the instruction stream to before the intermittent error and then re-execute the instructions.

The higher intrinsic reliability of a single-chip RISC processor, contrasted with the thousands of mainframe chips, diminished the demand for instruction retry in early RISC designs. However, a new problem has developed: As chip circuitry gets ever smaller with each process generation, electrical "noise" shows up, often caused by alpha particle radiation. Furthermore, since today's RISC systems are called upon for the most critical tasks, users demand mainframe-class reliability.

In its SPARC64 V implementation, Fujitsu becomes the first to offer mainframe-class hardware instruction retry in a RISC processor. For users, the benefit is avoiding system crashes due to intermittent errors. Hardware instruction retry is transparent to software and does not require any operating system or application support.

Except for a minuscule performance hiccup when the instruction is repeated, hardware instruction retry is not noticed, other than the crucial but positive fact that the system keeps running and does not crash from the intermittent failure. Eventually other chip design teams may learn to incorporate instruction retry; SPARC64's advantage is that Fujitsu has long developed such expertise and is shipping that capability now.

Fault isolation was also an important concern in early mainframe systems, which contained large numbers of replaceable components. By identifying the failing component, repairs could be accomplished quickly during assembly in the factory or at the customer's site. The evolution to integrated circuits now contains an entire RISC processor on a single chip. As a result, the ability to replace or repair portions of that single chip was lost. Furthermore, by eliminating most of the external wires and connectors, the highly integrated circuits were far less prone to failure. Therefore, typical RISC processors employed far fewer error detectors than older mainframes. Instead, available chip circuits were devoted to increasing performance rather than fault detection/isolation.

For example, typical RISC chip designs have focused on enhancing the performance of their execution units, and have not been inclined to insert error-checking circuits. Although failures may be relatively rare, the lack of error-checking circuits can mean that a hardware failure is never detected and leads to data corruption. Even if the bad data were discovered later, by that time it would be too late to reverse the erroneous execution and data corruption. The entire system would be typically brought down to avoid unknown data integrity exposures.

Fujitsu's mainframe-like solution is to trap errors when they first occur by adding extensive error checking to internal registers and data paths. In SPARC64 V, Fujitsu has added error checkers to processor registers, internal data paths, Arithmetic Logic Units (ALUs), data caches and tag arrays, and the Translation Lookaside Buffer (TLB). If the error is the result of a permanent failure, the SPARC64 V can disable portions of its circuitry, such as sections of the cache, without requiring intervention of software and can continue operating in a degraded mode.

Certainly, SPARC64 V offers error detection and correction for cache data and memory bus, as do many other current RISC processors. What sets SPARC64 V apart from other chips, and this is a benefit IT executives look for, is a mainframe-influenced level of error checking that avoids data integrity problems. All chip internal data paths are covered by parity to discover errors before they are written to cache. Execution units use parity prediction or residue checks – important mainframe techniques – to ensure the calculated result is not in error. Most of the architecturally defined registers and program-addressable registers are protected by parity. These additional levels of error detection and fault isolation may seem routine to mainframe designers, but are not commonplace in RISC designs. SPARC64 V leads the way with such mainframe-class techniques.

Review of Key Points

This white paper has highlighted some of the benefits of Fujitsu's SPARC64 V microprocessor implementation. Leveraging its experience in high-performance and highly available mainframes, Fujitsu designers have created a RISC chip that leads other implementations not only in performance, but also in error detection and correction. Using these new SPARC64 V processors, PRIMEPOWER offers state-of-the-art performance with mainframe-class error recovery, error isolation, and data integrity.

This white paper has also provided an overview of the SPARC64 V microprocessor, a key part of PRIMEPOWER's strong software and hardware foundation. This chip is the basis for PRIMEPOWER's ability to deliver best-in-class platform solutions to its customers.

Clearly, the combination of the SPARC64 V and the other technologies discussed in the other white papers in this series demonstrates that PRIMEPOWER is a short-list candidate for selection as a single SMP server or clustered SMP server operation in the business-critical IT infrastructure. The SPARC64 V microprocessor offers a powerful foundation, allowing PRIMEPOWER servers to deliver the highest levels of performance, availability, flexibility, scalability, and security. These are benefits that IT executives seek. Additional information concerning PRIMEPOWER's SPARC64 V and other PRIMEPOWER technology can be found on the Fujitsu websites.

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